Novel Fgmos Based Ultra Low-Power, High Frequency Half-Wave Rectifier

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Abstract— The work presents floating gate MOS (FGMOS) based low power, high frequency half wave (HW) rectifier. The basic principle of the winner-take-all (WTA) maximum circuit is exploited to obtain the desired structure. The HW rectifier takes a single sinusoidal signal as the input which is processed through WTA maximum circuit, and the output achieved is the positive swing of the input signal as expected. The simulations are performed using SPICE in 0.18µm CMOS technology with ±1.23V supply voltage to verify the operation of the proposed circuit. High frequency operation is achieved up to 300 MHz and the proposed circuit shows good temperature and noise stability and minimal variations in DC transfer characteristics for Monte Carlo simulations. The proposed rectifier is found to dissipate very low power of 0.328mW which makes it suitable for several low power applications.

Keywords— FGMOS, Half Wave Rectifier, Winner-Take-All, Low-Power, Analog Signal Processing

I. INTRODUCTION

Rectifiers are an important building block in analog and digital signal processing in particular for low level signals. Extensive applications of these circuits include RF demodulators, RMS to DC conversions, linear function generators, AC voltmeters, sample-and-hold circuits, peak detectors and nonlinear structures, to name a few. A conventional implementation of a rectifier is with diodes. However, the problem with this approach lies in the fact that such an implementation lacks the capability to rectify those signals whose amplitudes are less than the diode threshold voltage. A recent focus has been on the realization of rectifiers with the use of current conveyors as a building block. A wide technical literature relates to it [1-14] as current conveyors offer several advantages such as wider linearity, simpler architecture, larger dynamic range, wider bandwidths and low power consumption. In [1], design of FWR with the use of universal voltage conveyor and current conveyor is discussed. Implementation of full wave rectifier (FWR) from current differencing trans conductance amplifier (CDTA) as an alternative building block is presented in [15].The recent trends in consumer electronics have motivated researchers to develop low-voltage, low-power (LV/LP) circuits with their applications in analog signal processing. Among several LV/LP design techniques [16], FGMOS technique is seen to gather leading importance as it helps achieve the primary objectives of LV/LP circuit design and streamlining signal processing of complex antilog non-linear functions in addition to providing incredible features of controllability and tenability.

In our earlier work [17], we have reported new FGMOS based winner-take-all (WTA) maximum circuit. The circuit was presented as an improvement over its CMOS counterpart in terms of reduced supply voltage and power dissipation and can be employed in more interesting applications. This has been possible by the use of FGMOS transistors in these circuits. The transistor is known to offer several exclusive advantages and technology compatibility as well as exhibit versatility for use in many different fields as is well documented in [18]. It is because of these distinct features that several research publications relate to applications of FGMOS transistors in electronic programming [19] and neural networks [20]. Several FGMOS based analog signal processing circuits such as voltage controlled resistors [21], multipliers [22], squarer's [23], ADC/DACs [24] and current mirrors [25] have been recently proposed. FGMOS has also been used in the design of voltage mode active elements such as op-amps [26], operational transconductance amplifiers [27-30] and class AB output stage of CMOS op-amps [31]. As per authors' knowledge, FGMOS based structures of half wave rectifier were not found in existing literature.

Recently, CMOS technology based half wave rectifier has been presented [6], which essentially has three main components: a dual output V-I converter, two half-wave current rectifiers and two I-V converters. Advantages offered by the circuit are high operating frequencies up to 10 MHz, high accuracy and good temperature stability. Further, similar techniques were employed in [32], to propose a high frequency and high precision CMOS half-wave rectifier. High frequency performance of the circuit is achieved by employing CMOS class-AB current-mode rectifier. Several advantages offered by the circuit are high frequency operation up to 300 MHz, good temperature stability and high accuracy.

In this paper, FGMOS based structure of WTA maximum circuit is utilized to propose a novel structure of high frequency FGMOS based half wave rectifier based on winner-take-all algorithm. It needs special mention that the proposed rectifier uses similar architecture as in [33]; however the use of floating gate MOS transistors makes it more favourable from the

perspective of reduced supply voltage and power dissipation. The power dissipation of the proposed circuit is found to as minimal as 0.328mW. The workability of the proposed circuit is verified through SPICE simulations of 0.18µm CMOS technology. Several advantages offered by the proposed half wave rectifier are; use of 0.18µm process CMOS technology, high operating frequency, high operating range, good temperature stability and noise stability of the proposed circuits.

The paper is organized in the following manner; basics of FGMOS transistor are discussed in section 2. The FGMOS based WTA circuit is discussed in detail in section 3. Operation of the proposed rectifier is discussed in section 4. The simulation results are given in the subsequent section. Inferences from the results are drawn in the concluding section 6.

II. FLOATING GATE MOSFET (FGMOS)

A floating gate MOSFET is a device which is similar to the conventional MOSFET but differs in the sense that it has multiple inputs at the floating gate (FG) which are capacitive connected to it. The device does not have any resistive connections at the FG. The equivalent representation of n-input FGMOS is shown in Fig. 1.

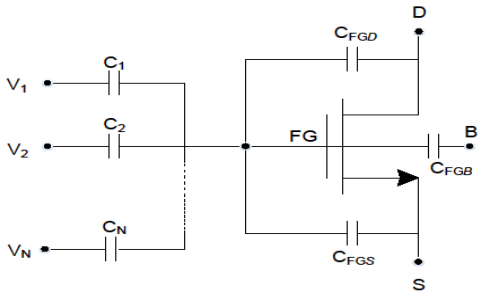


Fig.1: Equivalent Representation of FGMOS

The FG voltage can be appropriately interpreted as the weighted summation of all input voltages connected to the FG, the expression of which is given by [18],

$$V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i + \frac{C_{GS}}{C_T} V_S + \frac{C_{GD}}{C_T} V_D + \frac{Q_{FG}}{C_T} \qquad (1)$$

Here C_i is the set of capacitors associated with effective inputs and the floating gate. Here, the total floating gate capacitance,

$$C_T = \sum_{i=1}^{N} C_i + C_{FGS} + C_{FGD} + C_{FGB}$$

Where C_{FGD}, C_{FGS} and C_{FGB} are overlap capacitances of floating gate with drain, source and bulk, respectively, V_D is the drain voltage, V_S is the source voltage, V_B is the bulk voltage, and Q_{FG} is the residual charge trapped in the oxide-silicon interface during fabrication process. With the justification suggested in [23], neglecting residual charge, Q_{FG} and assuming $C_i >> C_{FGD}$, C_{FGB} [18], the drain current of FGMOS transistor operating in saturation region can be expressed by equation 2**.**

$$I_D = \frac{\beta}{2}\left(\sum_{i=1}^{N} \frac{C_i}{C_T} V_{iS} - V_T\right)^2 \qquad \ldots(2)$$

Here β is the trans conductance, V_T is the threshold voltage, V_{iS} is the gate to source voltage of inputs (in).

The DC characteristics of the device are obtained by employing the simulation model suggested in [18] to overcome the DC convergence error. This error occurs because the simulator cannot interpret the floating node and hence is unable to simulate. In this model, high value resistors are connected in parallel with capacitors. The simulation model of the 2-input FGMOS is described in the **Fig. 2**. The I-V characteristic of the 2-input FGMOS is shown in **Fig. 3**.

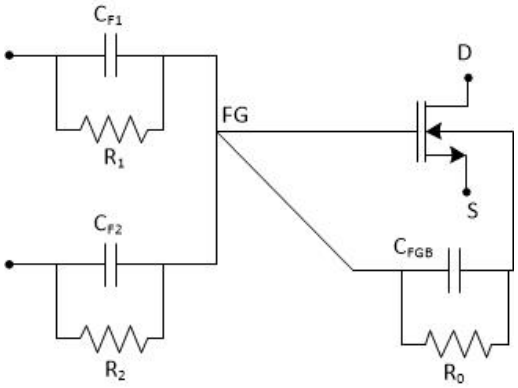


Fig.2: FGMOS Simulation Model

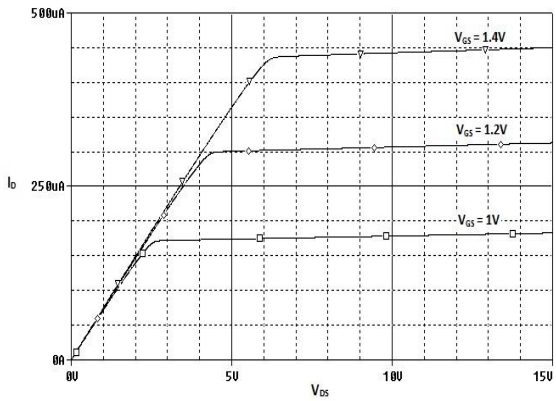


Fig.3: I-V Characteristics of 2-Input FGMOS

The drain current are obtained for V_{GS} = 1V, 1.2V and 1.4V while V_{DS} is varied from 0 to 15V. The transfer characteristics of the conventional MOSFET and the 2-input FGMOS is shown in **Fig. 4**. It is evident from this Fig. that the threshold voltage of the 2-input FGMOS is lower than that of the standard MOSFET. Effectively, the threshold of the device can be reduced further even to zero or negative value by incorporating more inputs at the FG. This advantage can be exploited for low voltage applications and in the development of tunable circuits for analog signal processing.

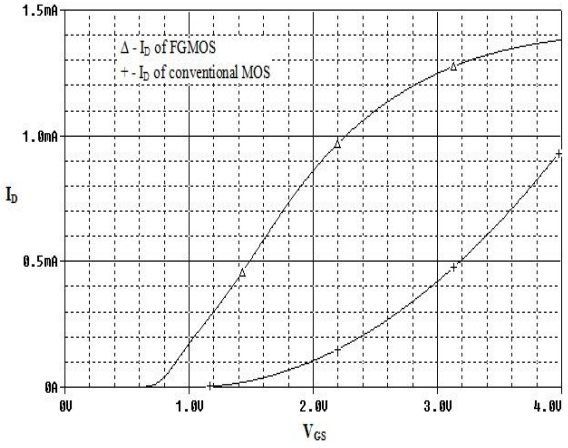


Fig.4: Comparison of Threshold Voltage of 2-Input FGMOS And Conventional MOSFET

III. CIRCUIT DESCRIPTION OF FGMOS BASED WTA

The symbol of the FGMOS based WTA circuit proposed previously in [17] is given in **Fig. 5** in which the output voltage is dominated by the maximum of the two input voltages. The schematic implementation of FGMOS based WTA Maximum circuit is shown in **Fig. 6**. The novel CMOS WTA maximum circuit previously proposed by Pipit Pommes and Kittikhun Chattrakun in [33] was improved in [17] by incorporating the use of FGMOS transistors to obtain a lower power alternative. The floating gate voltages V_{FG1} and V_{FG2} at FGs of M11 and M12 are given by The forcing condition of the current mirror (M_{3i} and M4) and the FGMOS voltage buffer ensures that only the winning transistor M_{1i} (i = 1 or 2) is operated based upon which floating gate voltage (V_{FG1} or V_{FG2}) is higher. Accordingly, the drain current of the corresponding winning transistor will be more than the drain current of the other transistor.

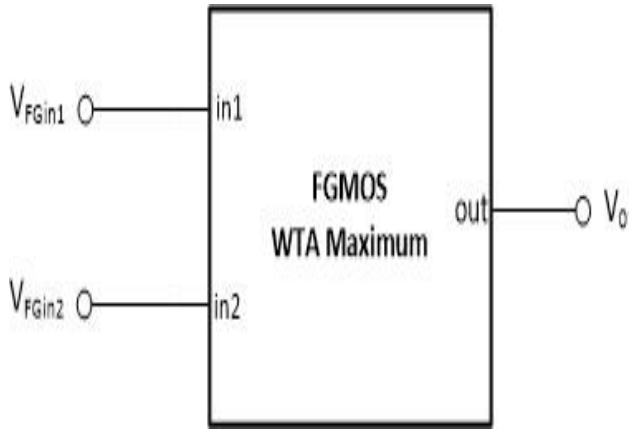


Fig.5: Symbolic Representation Of FGMOS WTA Maximum Circuit

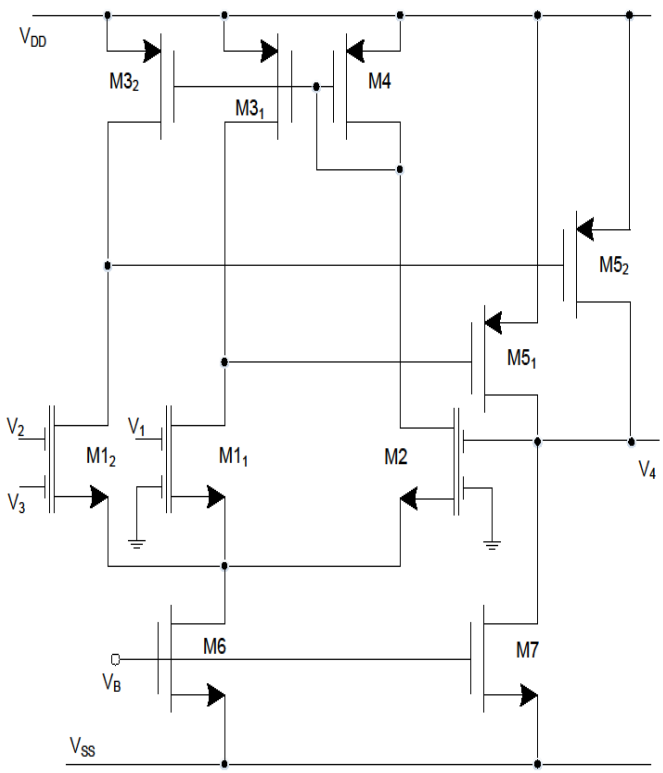


Fig.6: FGMOS Based WTA Maximum Circuit [17]

The circuit topology is based upon FGMOS voltage buffer proposed in [17]. The circuit configuration is shown in **Fig. 7**. The small signal equivalent circuit is given in **Fig. 8**.

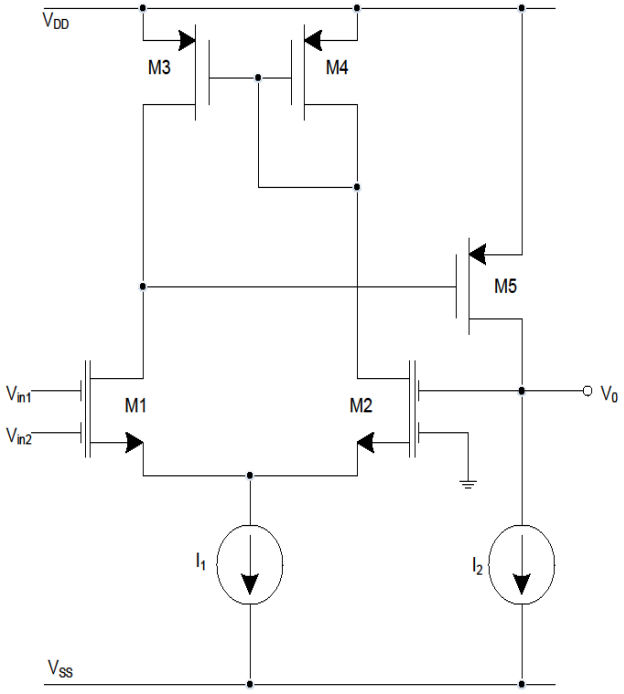


Fig.7: FGMOS voltage buffer[17]

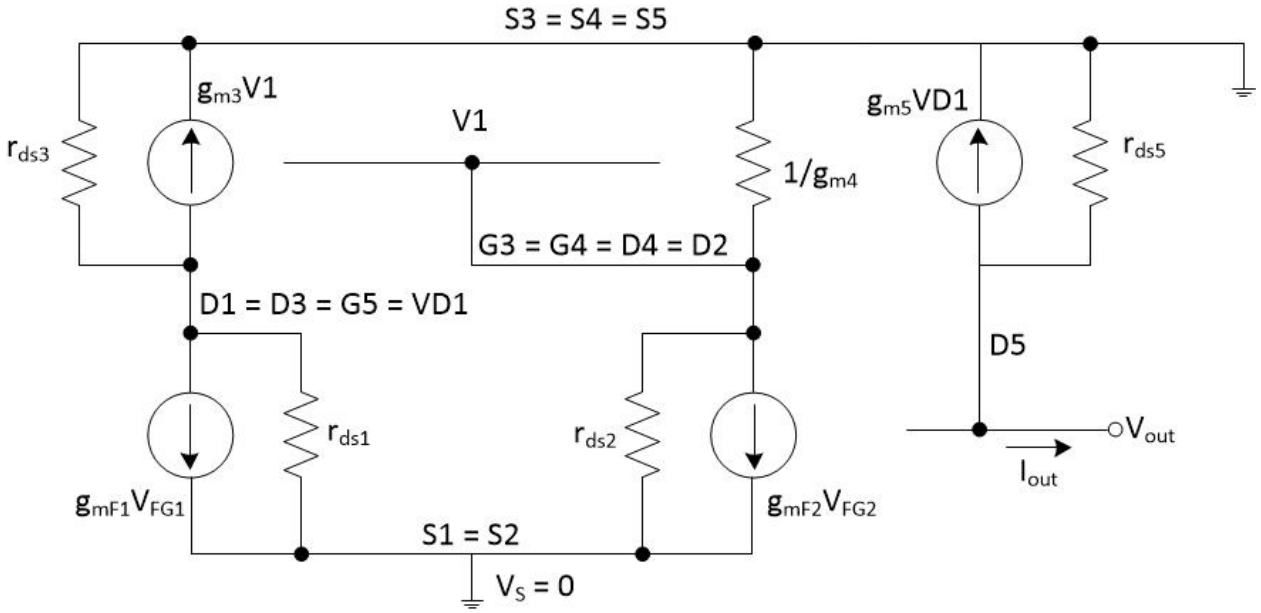


Fig.8: Small Signal Model Of FGMOS Based Voltage Buffer

The small signal equations for the FGMOS transistors, M1 and M2 are given by [18];
For M1,

$$g_{mF1} = \left(\frac{C_1}{C_{T_1}} + \frac{C_2}{C_{T_1}}\right) g_{m1} \quad \text{..... (3)}$$

$$g_{dsF1} = g_{ds1} + \frac{C_{GD1}}{C_{T_1}} g_{m1} \quad \text{.....(4)}$$

Similarly, for M2,

$$g_{mF2} = \left(\frac{C_3}{C_{T_2}} + \frac{C_4}{C_{T_2}}\right) g_{m2} \quad \text{..... (5)}$$

$$g_{dsF2} = g_{ds2} + \frac{C_{GD2}}{C_{T_2}} g_{m2} \quad \text{.....(6)}$$

Here, C_1, C_2 and C_3, C_4 are the floating gate capacitances at the floating gates of FGMOS M1 and M2. Also, g_{m1} and g_{ds1} are the gate transconductance and drain/output respectively of a MOS transistor having identical physical parameters as the FGMOS transistor M1. Similarly, g_{m2} and g_{ds2} are the gate transconductance and drain/output conductance respectively of a MOS transistor having identical physical parameters as the FGMOS transistor M2. The equivalent capacitances C_{T1} and C_{T2} are given as $C_{T1} = C_1 + C_2 + C_{GD1} + C_{GS1} + C_{GB1}$ and $C_{T2} = C_2 + C_2 + C_{GD2} + C_{GS2} + C_{GB2}$.

The FGMOS voltage buffer topology of **Fig. 7** resembles the topology of CMOS voltage buffer proposed in [33]. The small signal analysis of the circuit can be done to obtain expressions for input and output resistances. A high output resistance is observed at the input port which can be expressed as

$$r_{in} \approx \infty \quad \text{.....(7)}$$

Output resistance is obtained by setting the input, $V_{in1} = V_{in2} = 0$ and applying a test current source at the output terminal. Applying KCL at output node D5, we obtain

$$I_{out} = -g_{m5} V_{D1} - \frac{V_{out}}{r_{ds5}} \quad \text{..... (8)}$$

Since M3 and M4 act as current mirror, it can be assumed that drain voltages D3 and D4 are equal and hence V1 = VD1. Thus, (8) can be written as

$$I_{out} = -g_{m5} V1 - \frac{V_{out}}{r_{ds5}} \quad \text{..... (9)}$$

Now Applying KCL At Node V1, We Get

$$g_{mF2} V_{FG2} + \frac{V1}{\left(r_{ds2} || \frac{1}{g_{m4}}\right)} = 0 \quad \text{..... (10)}$$

Also, the floating gate voltage for transistor M2 is given by

$$V_{FG2} = \frac{C_3}{C_{T_2}} V_{out} \quad \text{..... (11)}$$

Substituting (11) in (10), we obtain

$$g_{mF2} \frac{C_3}{C_{T_2}} V_{out} + \frac{V1}{\left(r_{ds2} || \frac{1}{g_{m4}}\right)} = 0 \quad \text{.....(12)}$$

Thus, we obtain the expression of voltage at V1 as

$$V1 = -V_{out} \frac{C_3}{C_{T_2}} \left(r_{ds2} || \frac{1}{g_{m4}}\right) g_{mF2} \quad \text{.....(13)}$$

Substituting (13) in (9), we get

$$I_{out} = \left(g_{m5} g_{mF2} \frac{C_3}{C_{T_2}} \left(r_{ds2} || \frac{1}{g_{m4}}\right) - \frac{1}{r_{ds5}}\right) V_{out} \quad \text{.... (14)}$$

With$r_{ds2}||\frac{1}{g_{m4}}=\frac{r_{ds2}}{1+g_{m4}r_{ds2}}$, the expression for r_{out} is Obtained as

$$r_{out}=\frac{V_{out}}{I_{out}}=\frac{r_{ds5}+r_{ds2}r_{ds5}g_{m4}}{\frac{C_3}{C_{T2}}r_{ds2}r_{ds5}g_{mF2}g_{m5}-1-g_{m4}r_{ds4}} \quad \ldots\ldots(15)$$

r_{ds5} in the numerator can be neglected since $g_{m_{r0}} \gg 1$. Similarly the dominant term in the denominator is $\frac{C_3}{C_{T2}}r_{ds2}r_{ds5}g_{mF2}g_{m5}$. Thus, the equation is reduced as

$$r_{out}=\frac{C_{T2}}{C_3}\frac{g_{m4}}{g_{mF2}g_{m5}} \quad \ldots.. (16)$$

Also,

if $g_{m4}=g_{mF2}=g_{m5}=g_m$, we get

$$r_{out}=\frac{C_{T2}}{C_3}\frac{1}{g_m} \quad \ldots\ldots(17)$$

Now, $\frac{C_{T2}}{C_3}>1$. It can hence be inferred from the obtained expression that $r_{out}$is much on the lower side as it should exhibit for a voltage buffer. As per the simulation results mentioned in [17], the output resistance of FGMOS based voltage buffer is found to be 193Ω, in which case the circuit was simulated with 0.18µm CMOS technology.

IV. PROPOSED HALF WAVE RECTIFIER

The basic functionality of the WTA algorithm is exploited in the present proposal of half wave rectifier. The operation of the proposed rectifier is shown in **Fig. 9**. The basic principal block employed is the WTA maximum circuit. Multiple inputs can be provided by the use of FGMOS transistors M11 and M12. A sinusoidal waveform of variable frequencies and 500mV$_{peak}$ amplitude is fed as a signal processing input to the 2-input FGMOS transistor, while the other input of the transistor is grounded. Both inputs of the second FGMOS transistor are grounded. Voltage at the output of the proposed rectifier is described by equation 18.

$$V_0=\begin{cases}V_m sin\omega t, & V_{FGin1}>0\\ 0, & V_{FGin1}<0\end{cases} \quad \ldots..(18)$$

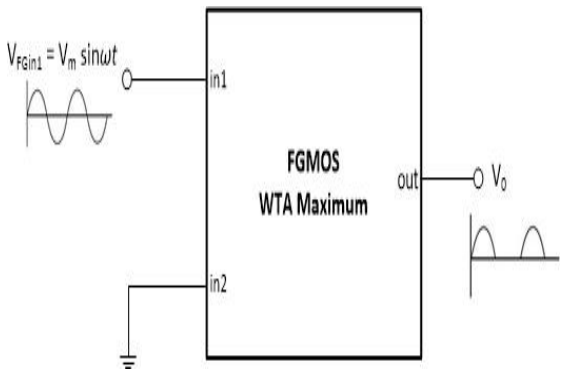


Fig.9: FGMOS WTA Half Wave Rectifier

V. SIMULATION RESULTS

To validate the theoretical design of the proposed rectifier, the circuit was simulated using PSPICE program with 0.18 µm CMOS technology. Model parameter of the process technology used for SPICE simulation is given in **Table. I**.

Table I: Level 7, 0.18 µm TSMC CMOS Parameters

.MODEL NMOS NMOS (LEVEL = 7 VERSION = 3.1
+TNOM = 27 TOX = 4.1E-9 XJ = 1E-7 NCH = 2.3549E17 VTH0 =0.3725327 K1 = 0.5933684
+K2 = 2.050755E-3 K3 = 1E-3 K3B = 4.5116437 W0 =+1E-7 NLX = 1.870758E-7+DVT0W=0 DVT1W=0 DVT2W=0 DVT0 = 1.3621338 DVT1 = 0.3845146 DVT2 = 0.0577255
+U0 = 259.5304169 UA=?1.413292E-9 UB = 2.229959E-18 UC = 4.525942E-11+VSAT = 9.411671E4 A0 = 1.7572867 AGS = 0.3740333
B0=?7.087476E-9 B1=?1E-7+KETA=?4.331915E-3 A1 =0 A2 = 1 RDSW= 111.886044 PRWG= 0.5
+PRWB=?0.2 WR= 1
+WINT = 0 LINT= 1.701524E-8 XL =0 XW=?1E-8 DWG=?1.365589E-8 DWB = 1.045599E-8
+VOFF=?0.0927546 NFACTOR = 2.4494296 CIT =0 CDSC= 2.4E-4 CDSCD =0 CDSCB= 0
+ETA0 = 3.175457E-3 ETAB = 3.494694E-5 DSUB = 0.0175288 PCLM = 0.7273497
+PDIBLC1 = 0.1886574 PDIBLC2 = 2.617136E-3 PDIBLCB=?0.1 DROUT = 0.7779462
+PSCBE1 = 3.488238E10 PSCBE2 = 6.841553E-10 PVAG = 0.0162206 DELTA = 0.01 RSH = 6.5
+MOBMOD = 1 PRT=0 UTE=?1.5 KT1=?0.11 KT1L =0 KT2 = 0.022 UA1 = 4.31E-9
+UB1=?7.61E-18 UC1=?5.6E-11 AT = 3.3E4 WL =0 WLN=1 WW= 0 WWN= 1
+WWL= 0
+LL = 0 LLN = 1 LW= 0 LWN= 1 LWL= 0 CAPMOD=2 XPART= 0.5 CGDO = 8.53E-10
+CGSO = 8.53E-10 CGBO = 1E-12 CJ = 9.513993E-4 PB = 0.8 MJ = 0.3773625
+CJSW = 2.600853E-10 PBSW = 0.8157101 MJSW = 0.1004233 CJSWG = 3.3E-10
+PBSWG = 0.8157101 MJSWG = 0.1004233 CF = 0 PVTH0=?8.863347E-4
+PRDSW=?3.6877287
+PK2 = 3.730349E-4 WKETA = 6.284186E-3 LKETA=?0.0106193 PU0 = 16.6114107
+PUA = 6.572846E-11 PUB = 0 PVSAT= 1.112243E3 PETA0 = 1.002968E-4
+PKETA=?2.906037E-3)

.MODEL PMOS PMOS (LEVEL = 7 VERSION = 3.1
+TNOM = 27 TOX = 4.1E-9 XJ = 1E-7 NCH = 4.1589E17 VTH0=?0.3948389
+K1 = 0.5763529 K2 = 0.0289236 K3 =0 K3B= 13.8420955 W0 = 1E-6 NLX = 1.337719E-7
+DVT0W=0 DVT1W=0 DVT2W=0 DVT0 = 0.5281977 DVT1 = 0.2185978 DVT2 = 0.1
+U0 = 109.9762536 UA = 1.325075E-9 UB = 1.577494E-21 UC=?1E-10 VSAT = 1.910164E5
+A0 = 1.7233027 AGS = 0.3631032 B0 = 2.336565E-7 B1 = 5.517259E-7 KETA = 0.0217218
+A1 = 0.3935816 A2 = 0.401311 RDSW = 252.7123939 PRWG= 0.5 PRWB= 0.0158894 WR = 1
+WINT = 0 LINT= 2.718137E-8 XL =0 XW=?1E-8 DWG=?4.363993E-8 DWB = 8.876273E-10
+VOFF=?0.0942201 NFACTOR =2 CIT= 0 CDSC= 2.4E-4 CDSCD = 0 CDSCB= 0
+ETA0 = 0.2091053 ETAB=?0.1097233 DSUB = 1.2513945 PCLM = 2.1999615
+PDIBLC1 = 1.238047E-3 PDIBLC2 = 0.0402861 PDIBLCB=?1E-3 DROUT = 0
+PSCBE1 = 1.034924E10 PSCBE2 = 2.991339E-9 PVAG = 15 DELTA = 0.01 RSH = 7.5
+MOBMOD = 1 PRT=0 UTE=?1.5 KT1=?0.11 KT1L =0 KT2 = 0.022 UA1 = 4.31E-9

+UB1=?7.61E-18 UC1=?5.6E-11 AT = 3.3E4 WL =0 WLN=1 WW= 0 WWN= 1 WWL= 0
+LL = 0 LLN = 1 LW= 0 LWN= 1 LWL= 0 CAPMOD=2 XPART= 0.5 CGDO = 6.28E-10
+CGSO = 6.28E-10 CGBO = 1E-12 CJ = 1.160855E-3 PB = 0.8484374 MJ = 0.4079216
+CJSW = 2.306564E-10 PBSW = 0.842712 MJSW = 0.3673317 CJSWG = 4.22E-10
+PBSWG = 0.842712 MJSWG = 0.3673317 CF = 0 PVTH0 = 2.619929E-3 PRDSW = 1.0634509
+PK2 = 1.940657E-3 WKETA = 0.0355444 LKETA=?3.037019E-3 PU0=?1.0227548
+PUA=?4.36707E-11 PUB = 1E-21 PVSAT=?50 PETA0 = 1E-4 PKETA=?5.167295E-3)

The aspect ratios of the transistors used in simulations for the Proposed rectifiers are provided in the Table. II.

Table. II: Aspect Ratios of the Transistors of Proposed Rectifier

Transistors	W(µm)	L(µm)
M11, M12, M2	1	0.25
M31, M32, M4, M51, M52	5	0.25
M6, M7	3	0.25

The supply voltages used are ±1.23V. The DC transfer characteristics of the proposed rectifier are shown in **Fig. 10**, which shows the operating voltage range from 0 to 1.23V of the input voltage. It is observed that the operation of the proposed single output rectifier is well justified in the positive supply voltage range 0 to 1.23V as expected. Intuitively, the input range of the proposed circuit should increase because of the use of FGMOS transistors in which the equivalent capacitance ratio (C_i/C_T) scales down the effective input signal at the FG. A comparison of the operating range of the circuit with the previously proposed half wave rectifiers suggests a significant increase. The comparison is done for single output voltage. It needs special mention that the use of FGMOS in the proposed rectifiers has indeed increased the operation range compared to the previously proposed rectifiers. This is evident from the comparative analysis done in **Table III**. The power dissipation is found to 0.328mW for the proposed rectifier. The proposed rectifier is found to operate at high frequency inputs. The applied sinusoidal signal has input of amplitude $500mV_{peak}$ having frequencies 100 kHz, 1 MHz, 10 MHz, 100 MHz, 200 MHz and 300 MHz. The transient response of the proposed rectifier at different frequencies is shown in Fig. **11(a-f)**.

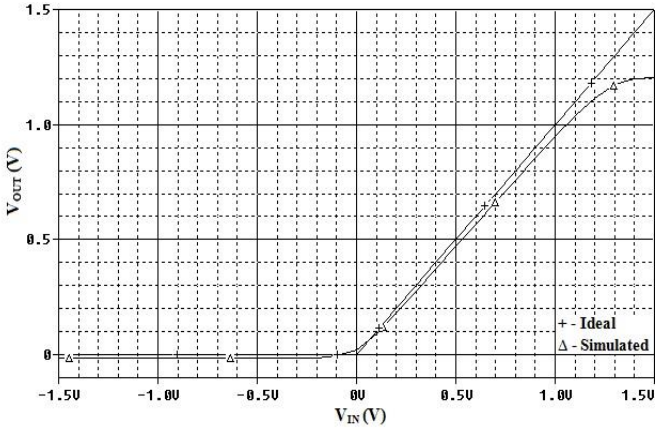
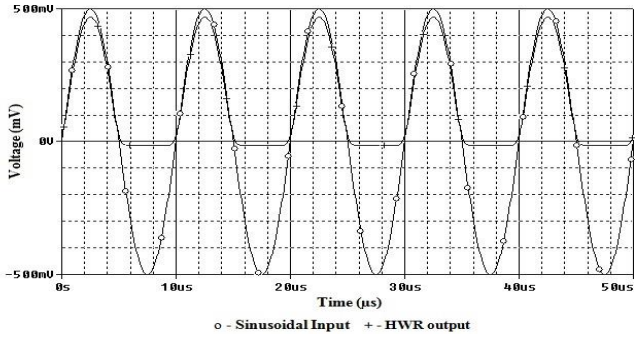
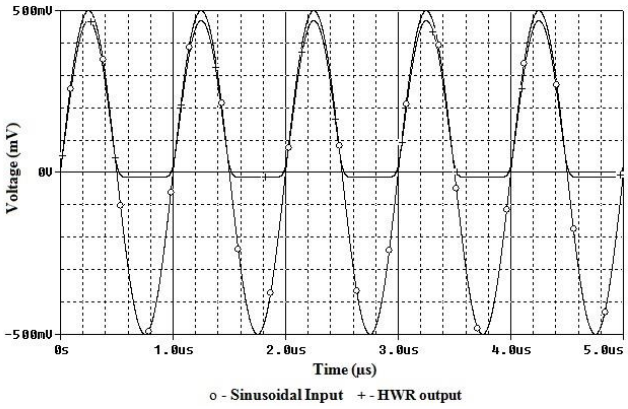


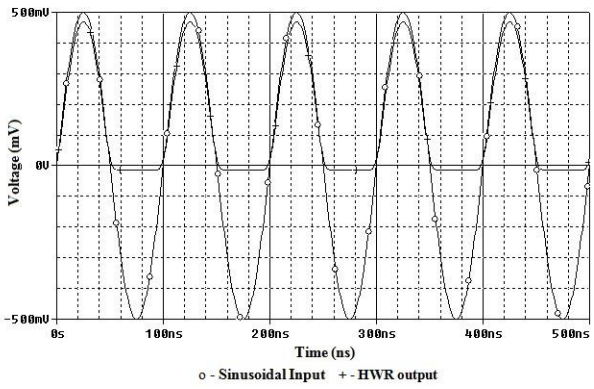
Fig.10: DC Transfer Characteristic of Proposed Rectifier



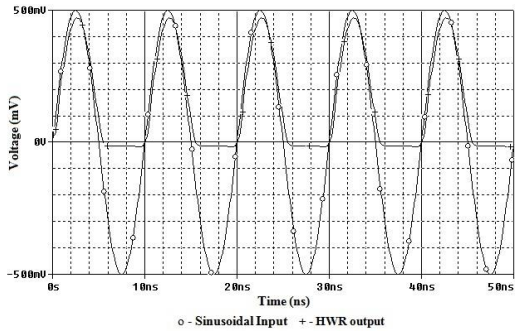
(a): 100 kHz



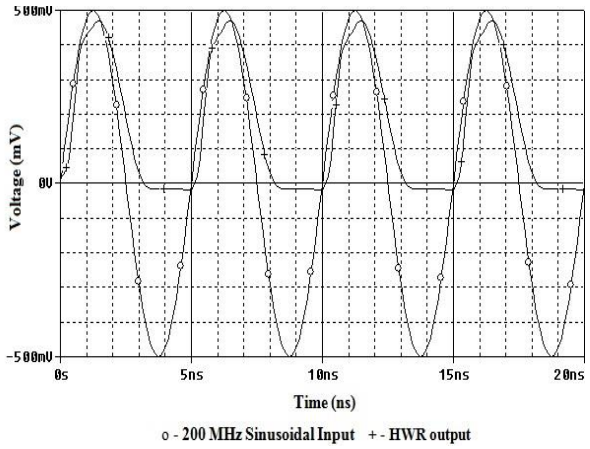
(b): 1 MHz



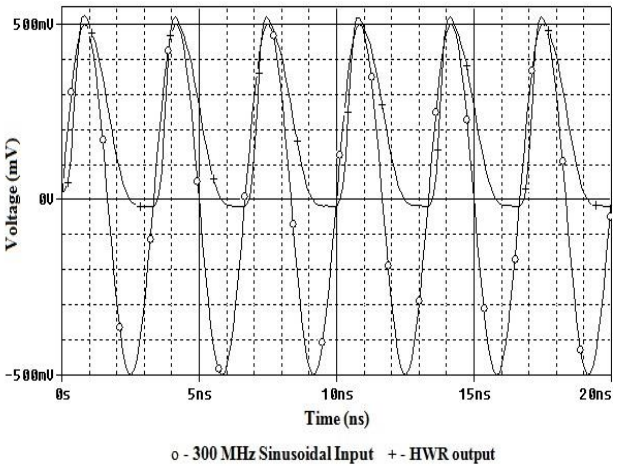
(c): 10 MHz



(d): 100MHZ



(e): 200 MHz



(f): 300 MHz

Fig.11(A-F): Sinusoidal Input And Rectified output of The Proposed Rectifier At Different Frequencies

Noise analysis of the proposed rectifier achieves good results. In **Fig. 12**, the level of output noise simulation is 320.5 nV/√Hz at 1 kHz. This decreases to 28.637 nV/√Hz at 100 MHz However, there is a slight increase in the output noise at around 1 GHz. The increase is observed up to 72.862 nV/√Hz at 1.6 GHz and for the following frequencies a decline in the noise output voltage is observed.

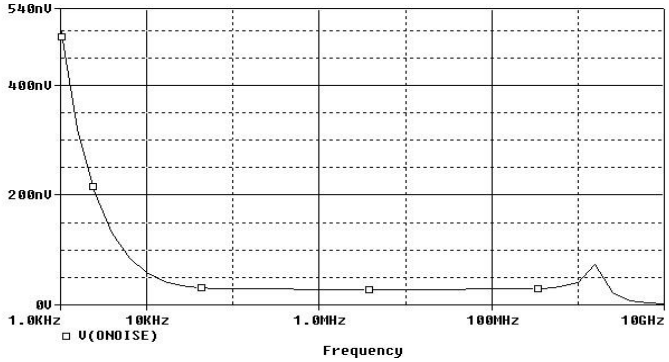


Fig.12: Output Noise Spectral Density vs Frequency for the proposed rectifier

The total RMS output noise vs frequency for the proposed rectifier is shown in the **Fig. 13**. The total simulated output noise at 27°C over a bandwidth of 10 MHz is 91.8 µV RMS. The higher measured noise levels could be a result of the circuit's quiescent power dissipation. Overall the simulated noise model gives excellent results.

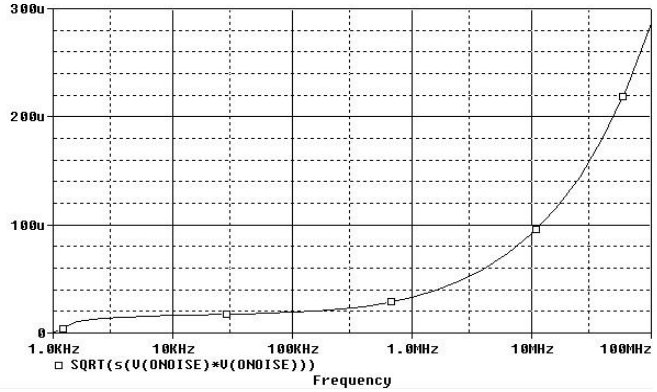


Fig.13: Total RMS Output Noise versus Frequency for The Proposed Rectifier

The performance of the proposed rectifier is checked at variable temperatures ranging from 0°C, 27°C, 50°C, 75°C and 100°C. The DC transfer characteristics at these temperatures simulated results at 100 MHz are shown in **Fig. 14**. The circuit is thus known to offer good temperature stability as per simulation results.

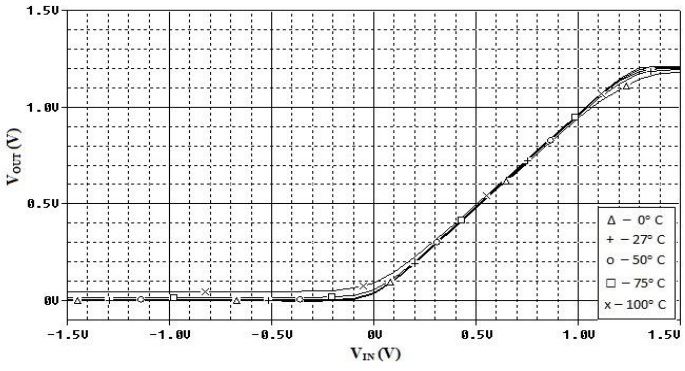


Fig.14: DC Transfer Characteristic of the Proposed Rectifier at Different Temperatures

Monte Carlo analysis was done to observe the variation of DC response of the proposed half wave rectifier. The simulation results performed for 20% deviation in the capacitors of the floating gate transistors with Gaussian distribution function give satisfying results. The simulation was carried out for 100 runs. The traces of all simulation runs are almost overlapping and hence indistinguishable as desired. The output of simulation is shown in Fig. 15.

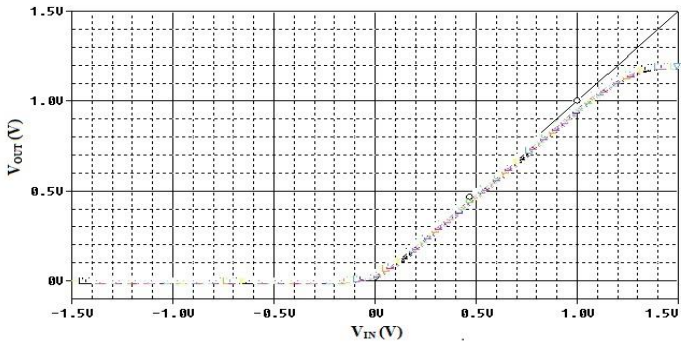


Fig.15: Monte Carlo Simulation with 100 Runs for DC Transfer Characteristic of Proposed Rectifier With 20% Deviation In Capacitances Of FGMOS Transistors.

The effect of threshold voltage of the floating gate transistors is also studied through Monte Carlo analysis. The simulation is carried out for 50 runs. For a 2% uniform distribution deviation in the threshold voltage of the FGMOS transistors, the simulation results for the DC transfer characteristic of the proposed half wave rectifier gives the output shown in **Fig. 16**. In this case also, the traces of all simulation runs are almost overlapping as desired only showing slight variation which is accounted for the deviation.

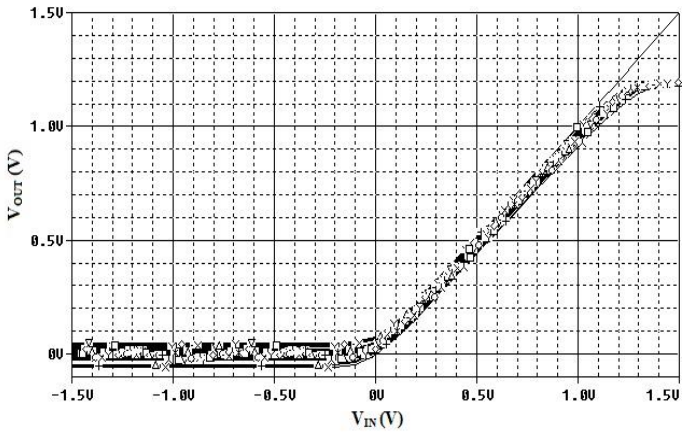


Fig.16: Monte Carlo Simulation with 50 Runs for Dc Transfer Characteristic of Proposed Rectifier With 2% Deviation In Threshold Voltage of FGMOS Transistors

SPICE simulations were done to perform Fourier analysis of the output signal with fundamental frequency of 1 kHz. The total harmonic distortion for the proposed rectifier is found to be 1.76%. **Fig. 17** shows the frequency response of the output voltages of the proposed rectifiers. A 3dB bandwidth of 720.374MHz is achieved in the case of the proposed rectifier.

Table III Comparison Of The Proposed Circuits With Previous Works

	Technology (µm)	Supply voltage (V)	Power consumption (mW)	Operation range with applied sine wave amplitude	-3dB band width (MHz)	Highest operating frequency (MHz)
[33]	0.25	±1.25	0.62	-	-	5
[34]	0.5	±1.2	1	-0.3V to +0.3V at 0.6V_{peak}	34.33	100
[2]	0.5	±1.2	-	-0.5V to +0.5V at 0.1V_{peak}	-	100
[35]	0.5	±5	-	-0.5V to +0.5V at 0.2V_{peak}	-	200
[9]	0.35	±2.5	-	-0.35V to +0.35V at 0.35V_{peak}	83	32
[10]	0.5	±2.5	-	-1V to 1V at 0.2V_{peak}	-	1
[36]	0.18	±2.4	0.825	-0.3V to +0.3V at 0.3V_{peak}	-	1000
[6]	0.5	±1.2	1.8	-0.3V to +0.3V at 0.1V_{peak}	-	100
[32]	0.5	±1.2	1.76	-0.25V to 0.25V at 0.2V_{peak}	333	300
Proposed	**0.18**	**±1.23**	**0.328**	**0 to 1.23V at 0.5V_{peak}**	**720**	**300**

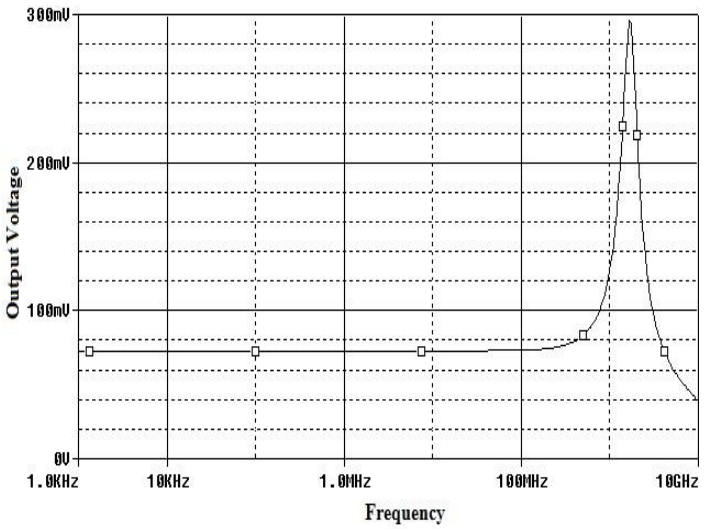


Fig.17: Frequency response of output voltage of the proposed rectifier

VI. CONCLUSIONS

In the present work, efficient structures of high frequency FGMOS based half wave and full-wave rectifiers were obtained in terms of lower supply voltages and reduced power consumption. The proposed rectifiers achieve high frequency operation at a supply voltage of ±1.23V at 0.18µm CMOS technology. The operation frequency achieved is as high as 300MHz. The proposed rectifier uses the comparison principal of the robust WTA algorithm. Power dissipation is found to extremely low as compared to previously prosed circuits. In addition, the circuit exhibits excellent noise and temperature stability. It is thus suitable for the regular rectifier applications and in other low-power, high-frequency operations in many analog signal processing circuits.

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