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# Design and Optimization of Reversible SR and JK Flip-Flops Using Qiskit for Quantum Noise Analysis

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**Abstract: Reversible logic preserves information through one-to-one input–output mappings, but a reversible memory element must also reproduce its state-transition behavior under that constraint. This paper presents reversible SR and JK flip-flop circuits built from Feynman, Peres and Fredkin gates and implemented in IBM Qiskit. Each design is derived from its characteristic equation and verified for all eight combinations of present state and inputs. The SR circuit uses three Feynman gates and one Peres gate, with quantum cost 7, two garbage outputs and depth 6. The JK circuit uses two Fredkin gates and two Feynman gates, with quantum cost 12, three garbage outputs and depth 11, one unit below the cost of 13 reported for the reference JK design. Both circuits were then simulated under bit-flip, depolarizing, amplitude-damping and phase-damping noise applied after every gate, using 4096 shots for each of the eight inputs. With a per-gate error probability of 0.02, the SR circuit returned the complete correct output vector in 72.9%, 85.0% and 84.2% of shots under bit-flip, depolarizing and amplitude-damping noise, against 61.6%, 77.9% and 75.8% for the JK circuit. The gap follows the number of noisy gate operations in each circuit. Phase damping had no effect on either circuit because every state involved is a computational-basis state. The one-unit cost saving of the JK design therefore comes with a larger noise exposure than the SR design, and the results give a reproducible baseline for noise-aware reversible sequential design.**

***Keywords:*** *Reversible Logic, SR Flip-Flop, JK Flip-Flop, Qiskit, Quantum Cost, Garbage Outputs and Quantum Noise.*

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## I. INTRODUCTION

Reversible logic has drawn steady interest in low-power computing and quantum circuit design. A reversible circuit has a one-to-one correspondence between its complete input and output vectors, so the inputs can always be recovered from the outputs. Landauer linked the loss of information to heat dissipation, and Bennett showed that computation can in principle be carried out without such loss [1], [2]. Logical reversibility does not by itself guarantee low energy use in a physical device, but it is a necessary property of every quantum circuit, which is why reversible designs are a natural starting point for quantum hardware.

Memory elements are essential to any digital system, and SR and JK flip-flops are the most familiar of them. The SR flip-flop sets, resets or holds its state, but it has a forbidden input when S and R, are asserted together. The JK flip-flop removes that restriction by toggling when J and K are both high. Making these devices reversible is not straightforward, because their state-update functions map three inputs to one output and so cannot be one-to-one as they stand. Extra constant inputs and retained garbage outputs are needed to restore reversibility, and every extra gate adds to the cost.

Reversible sequential circuits have been studied for some time. Thapliyal and Ranganathan designed latches and flip-flops that are optimized for quantum cost, delay and garbage outputs, and their results are widely used as a reference [3], [4]. Earlier work on reversible synthesis of sequential circuits [5], designs aimed at transistor-level feasibility [6] and synthesis methods for reversible sequential elements [7] cover related ground, and a recent study has examined quantum implementations of reversible latches [8].

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In most of this literature the circuits are compared by quantum cost, delay and garbage outputs, usually from hardware-description-language simulation, and their behavior under noise is not examined.

This paper takes a complementary route. The SR and JK circuits are implemented gate by gate in IBM Qiskit [9], derived from their characteristic equations, and checked against those equations for every combination of present state and inputs. Their cost, depth and garbage outputs are reported under conventions that are stated explicitly, and both circuits are then simulated under four noise models to see how much of the ideal behavior survives. Section II defines the gates and metrics, Section III develops the mathematical model, Section IV presents the circuits, and Section V reports the verification and resource analysis. Section VI describes the noise study, Section VII compares the designs with the reference, and Section VIII concludes.

The contributions of this work are fourfold. First, gate-level Qiskit realizations of reversible SR and JK next-state functions are given, with the SR design built from three Feynman gates and one Peres gate and the JK design from two Fredkin gates and two Feynman gates. Second, both designs are verified exhaustively over all eight input and present-state combinations, including the design-defined hold response of the SR circuit at S = R = 1 and the toggling response of the JK circuit at J = K = 1. Third, quantum cost, garbage outputs, delay and circuit depth are derived explicitly, and the JK circuit lowers the reference quantum cost from 13 to 12 while the SR circuit only matches the reference. Fourth, both circuits are evaluated under four noise channels applied after every gate for all eight inputs, which shows that a small cost saving does not guarantee better noise tolerance.

## II. REVERSIBLE GATES AND METRICS

➢ *Reversible Gates*

A circuit with *n* inputs and *n* outputs is reversible when its mapping is a bijection, as in (1). Three standard gates are used here: the Feynman gate (FG) [10], the Fredkin gate (FRG) [11] and the Peres gate (PG) [12]. Throughout, ⊕ denotes XOR, juxtaposition denotes AND, and a prime denotes complement.

$$F: \{0,1\}^{//n//} \rightarrow \{0,1\}^{//n//}, \text{ one-to-one and onto} \quad (1)$$

The FG is a controlled-NOT, given in (2). The PG combines a Toffoli gate and a CNOT, given in (3). The FRG is a controlled swap, given in (4); when its first input is held at 1 it simply exchanges the other two inputs. Their quantum costs are 1, 4 and 5 respectively [4]. Fig. 1 to Fig. 3 show each gate as a block and as the Qiskit circuit used in this work.

$$\text{FG: } (A, B) \rightarrow (A, A \oplus B) \quad (2)$$

$$\text{PG: } (A, B, C) \rightarrow (A, A \oplus B, AB \oplus C) \quad (3)$$

$$\text{FRG: } (A, B, C) \rightarrow (A, A'B + AC, AB + A'C) \quad (4)$$

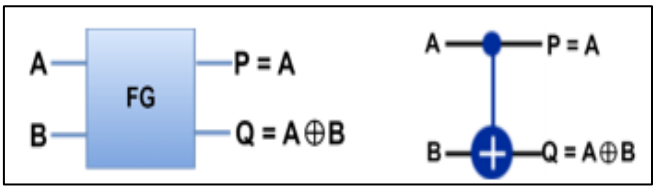


Fig 1 Feynman Gate: (a) Block, (b) Qiskit Circuit.

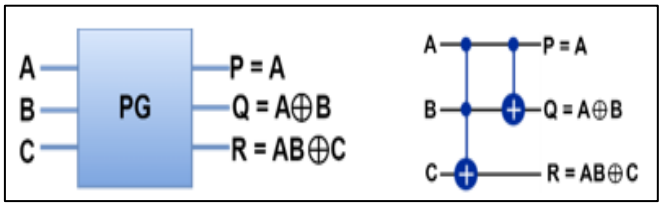


Fig 2 Peres Gate: (a) Block, (b) Qiskit Circuit.

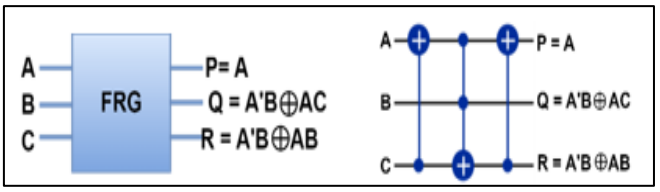


Fig 3 Fredkin Gate: (a) Block, (b) Qiskit Circuit (CNOT–Toffoli–CNOT).

➢ *Evaluation Metrics*

Quantum cost is the sum of the costs of the gates in a circuit, as in (5). Delay is expressed in units Δ with each gate's delay equal to its quantum cost [4]. Circuit depth is the number of layers in the Qiskit circuit when every operation, including single-qubit X and T gates, CNOT and Toffoli gates, counts as one. Garbage outputs are outputs that carry no required function, and constant inputs are inputs fixed to 0 or 1. When a design is compared with a reference, the relative saving in quantum cost is given by (6).Delay and depth are different metrics: delay weights each gate by its quantum cost, so it equals the quantum cost under this convention, whereas depth counts layers of the Qiskit circuit and treats every operation as one regardless of its cost. A circuit with a low delay can therefore still have a large depth, and the two values should not be compared directly.

$$QC = \sum_i QC_i \quad (5)$$

$$\text{Reduction (\%)} = (QC_{ref} - QC_{prop}) / QC_{ref} \times 100 \quad (6)$$

## III. MATHEMATICAL MODEL

➢ *Characteristic Equations*

With present state $Q_t$, the SR flip-flop follows (7), subject to $SR = 0$, and the JK flip-flop follows (8). Table I lists the resulting behavior.

$$Q_{t+1} = S + R'Q_t, \quad SR = 0 \quad (7)$$

$$Q_{t+1} = J \; Q_t' + K' \, Q_t \quad (8)$$

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Table 1 Next-State Behavior

| S / J | R / K | SR: Q(t+1) | JK: Q(t+1) |
|---|---|---|---|
| 0 | 0 | Q(t) | Q(t) |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | forbidden | Q(t)′ |

The input pair S = R = 1 is undefined in the conventional SR flip-flop. In the reversible circuit of Section IV, the pair is assigned the hold operation, $Q_{t+1} = Q_t$. This is a choice made in the design, not a property of the conventional device, and Section V reports it separately.

➢ *Reversible Embedding*

The maps from (S, R, $Q_t$) and from (J, K, $Q_t$) to $Q_{t+1}$ have three inputs and a single output, so neither is one-to-one. A reversible circuit has to keep enough extra information that the complete output vector identifies the complete input vector. The circuits in the next section do this with constant inputs and garbage outputs. A characteristic equation therefore says nothing about reversibility on its own, and in Section V the complete output vectors of every circuit are checked to be distinct.

*A. Proposed Circuits*

The proposed reversible SR and JK flip-flop circuits are developed using Feynman (FG), Peres (PG), and Fredkin (FRG) gates, with particular emphasis on their state-transition functionality, reversible signal routing, quantum resource requirements, and behavior under quantum noise.

➢ *Proposed Reversible SR Flip-Flop Architecture*

The SR flip-flop employs three Feynman gates and one Peres gate. The first Feynman gate produces the intermediate signal R ⊕ S while the second produces S ⊕ Qt. The Peres gate uses these intermediate signals to implement the reversible next-state transformation:

$$Q_{t+1} = Q_t \oplus (S \oplus Q_t)(R \oplus S) \quad (9)$$

The final Feynman gate generates the complementary state output. The resulting circuit requires four qubits, has a quantum cost of 7, produces two garbage outputs, and has a circuit depth of 6. Unlike the conventional SR characteristic function, which treats (S=R=1) as a forbidden condition, the proposed reversible implementation explicitly assigns a hold operation to this input combination. This extension provides a deterministic output for all eight input and present-state combinations. The hold convention is an implementation decision rather than a modification to the standard SR flip-flop specification.

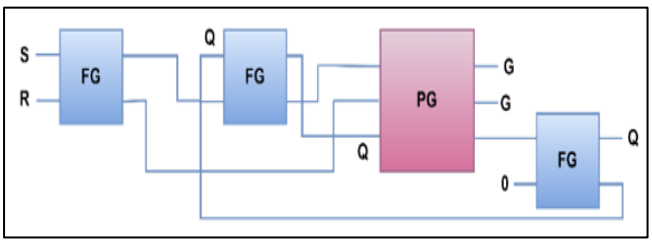



Fig 4 Proposed SR Flip-Flop Built from FG and PG Gates.

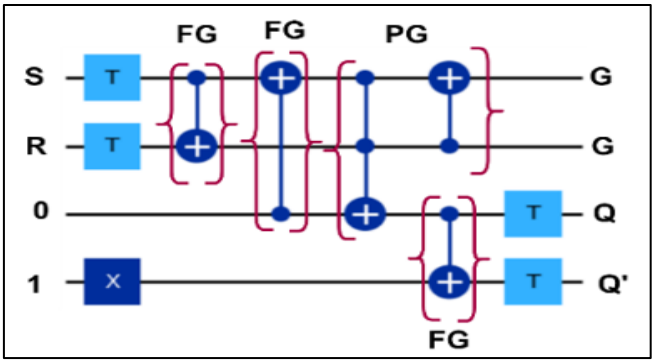



Fig 5 Qiskit Circuit of the SR Flip-Flop. The Third Input is the Present State $Q_t$, Shown as 0 for the All-Zero Case.

➢ *Proposed Reversible JK Flip-Flop Architecture*

The JK flip-flop uses two Fredkin gates and two Feynman gates. Its next-state function is expressed as:

$$Q_{t+1} = Q_t' J + Q_t K' \quad (10)$$

The first Fredkin gate directly realizes this expression through conditional data selection controlled by the present state. The second Fredkin gate, with a constant control input, provides reversible signal routing. The Feynman gates generate the required normal and complementary outputs. This arrangement has a quantum cost of 12, compared with the cost of 13 reported for the reference JK implementation in [4], representing a 7.69% reduction under the adopted quantum-cost convention. The circuit produces three garbage outputs and has a depth of 11.

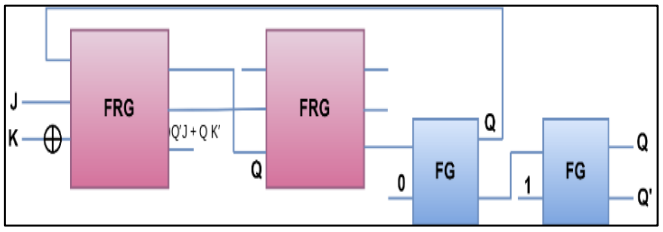



Fig 6 Proposed JK Flip-Flop Built from FRG and FG Gates.

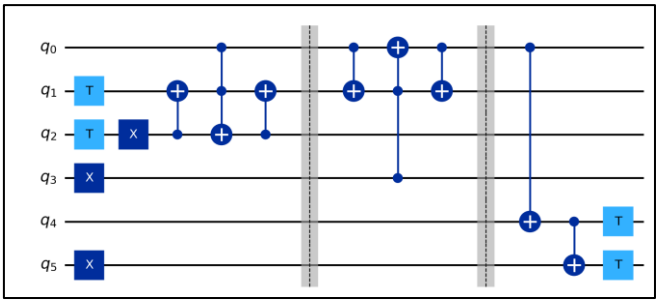



Fig 7 Qiskit Circuit of the JK Flip-Flop: $q_0 = Q_t$, $q_1 = J$, $q_2 = K$ (Inverted by the X Gate), $q_3 = 1$, $q_4 = 0$ (Output Q) and $q_5 = 1$ (Output Q′).

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The proposed work contributes a gate-level Qiskit realization of both reversible state-transition functions, exhaustive functional verification, explicit accounting of quantum resources, and a comparative investigation under bit-flip, depolarizing, amplitude-damping, and phase-damping noise channels. The proposed SR architecture matches the reference circuit in quantum cost and garbage-output count; therefore, no resource improvement is claimed for those metrics. The JK implementation achieves a modest reduction in reported quantum cost without reducing the number of garbage outputs. Although the selected gate configurations are described mathematically and evaluated experimentally through simulation, their architectural uniqueness relative to individual earlier circuit topologies must be established through direct gate-level comparison. Consequently, the principal contribution is the combined implementation, verification, resource evaluation, and noise characterization, together with the reported JK quantum-cost reduction.

## IV. COMPREHENSIVE FUNCTIONAL VERIFICATION OF REVERSIBLE SR AND JK FLIP-FLOPS

➢ *Functional Verification Methodology*

The functional correctness of the proposed reversible SR and JK flip-flop architectures was evaluated using IBM Qiskit and the Aer simulator. Both circuits were examined for all eight possible combinations of their two control inputs and the present state, Q(t). The verification procedure involved initializing the input and ancillary qubits, executing the reversible gate network, measuring the resulting computational-basis states, and comparing the measured next-state outputs with the theoretically expected characteristic equations.

The reported ideal simulations used 1,024 measurement shots for each input combination. Both circuits produced deterministic measurement outcomes consistent with their specified next-state functions.

In addition to verifying Q(t+1), the analysis examined the complementary output Q'(t+1) and the complete measured output vector. The latter provides an additional check that different input combinations remain distinguishable in the reversible implementation.

➢ *Mathematical Verification of the SR Flip-Flop*

The conventional SR flip-flop is a fundamental sequential logic element that stores a single binary state using two control inputs, namely Set (S) and Reset (R). Its next-state behavior depends on the present state and the applied input combination. The characteristic equation of a conventional SR flip-flop is expressed as

$$Q(t+1) = S + R'Q(t), \text{ for } SR = 0 \quad (11)$$

Where (Qt) represents the present state, $Q_{\{t+1\}}$ denotes the next state, and (\overline{R}) indicates the complement of the reset input.

The proposed reversible implementation uses:

$$Q(t+1) = Q(t) \oplus [(S \oplus Q(t))(R \oplus S)] \quad (12)$$

Here, $\oplus$ represents the XOR operation. The implementation is verified under four operating conditions:

- *Case 1: S = 0, R = 0 (Hold)*

The next state remains equal to the present state:

$Q(t+1) = Q(t)$.

- *Case 2: S = 0, R = 1 (Reset)*

The next state becomes zero, irrespective of the previous state:

$Q(t+1) = 0$.

- *Case 3: S = 1, R = 0 (Set)*

The next state becomes one, irrespective of the previous state:

$Q(t+1) = 1$.

- *Case 4: S = 1, R = 1 (Design-defined hold)*

In a conventional SR flip-flop, simultaneous activation of the set and reset inputs is forbidden. The proposed circuit resolves this otherwise undefined input combination by assigning:

$Q(t+1) = Q(t)$.

This behavior is explicitly defined for the proposed implementation and should not be interpreted as the standard response of a conventional SR flip-flop.

Both circuits were built in Qiskit 2.6.1 and run on the Aer simulator for all eight combinations of present state and inputs, with 1024 shots each. All gates in the circuits permute computational-basis states, so every run returned a single outcome with probability one, and the T gates only add phase and do not change those outcomes. Each result was compared with the characteristic equation, and reversibility was checked by confirming that the eight complete output vectors of each circuit are distinct. The measurement register has seven classical bits, and the bits above the highest qubit remain zero.

For the SR circuit, S = 0, R = 0 holds the state, S = 0, R = 1 resets it to 0, and S = 1, R = 0 sets it to 1, as Eq. (9) requires. The forbidden pair S = R = 1 returns Q(t+1) = Q(t) because R $\oplus$ S = 0 removes the product term, so the hold response is deterministic for both values of Q(t) (rows 7 and 8 of Table II). For the JK circuit, J = K = 0 holds the state, J = 0, K = 1 resets it, J = 1, K = 0 sets it, and J = K = 1 toggles it, giving Q(t+1) = 1 for Q(t) = 0 and Q(t+1) = 0 for Q(t) = 1 (rows 7 and 8 of Table III), in agreement with Eq. (10).

Table 2 and Table 3 show the outcomes. Every row of both tables agrees with the characteristic equations, with the S = R = 1 rows of the SR circuit following the hold convention of Section III. The eight output vectors are distinct in each circuit, so both mappings are reversible.

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Table 2 Verification of the SR Circuit

| S | R | Q(t) | Q(t+1) | Q′ | Output |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0001000 |
| 0 | 0 | 1 | 1 | 0 | 0000101 |
| 0 | 1 | 0 | 0 | 1 | 0001011 |
| 0 | 1 | 1 | 0 | 1 | 0001010 |
| 1 | 0 | 0 | 1 | 0 | 0000110 |
| 1 | 0 | 1 | 1 | 0 | 0000111 |
| 1 | 1 | 0 | 0 | 1 | 0001001 |
| 1 | 1 | 1 | 1 | 0 | 0000100 |

Table 3 Verification of the JK Circuit

| J | K | Q(t) | Q(t+1) | Q′ | Output |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0101100 |
| 0 | 0 | 1 | 1 | 0 | 0011011 |
| 0 | 1 | 0 | 0 | 1 | 0101000 |
| 0 | 1 | 1 | 0 | 1 | 0101010 |
| 1 | 0 | 0 | 1 | 0 | 0011101 |
| 1 | 0 | 1 | 1 | 0 | 0011111 |
| 1 | 1 | 0 | 1 | 0 | 0011001 |
| 1 | 1 | 1 | 0 | 1 | 0101110 |

Table 4 summarizes the resources of the two circuits. Depth was recomputed from the Qiskit circuits under the convention of Section II, and the SR and JK values are 6 and 11. The SR circuit needs four qubits and the JK circuit six.

Quantum cost follows from Eq. (5) with the gate costs of Section II-A. The SR circuit costs $3 \times 1 + 4 = 7$ and the JK circuit $2 \times 5 + 2 \times 1 = 12$. With each gate delay equal to its quantum cost, the delays are $7\Delta$ and $12\Delta$. The SR circuit has two garbage outputs, which are the Peres-gate outputs $R \oplus S$ and $Q(t) \oplus R$. The JK circuit has three, namely the retained present state, the second output of the first Fredkin gate, and the constant 1 returned by the second Fredkin gate. Depth was read from the Qiskit circuits as constructed, with every X, T, CNOT and Toffoli operation counted as one layer, giving 6 for the SR circuit and 11 for the JK circuit.

Table 4 Resource Summary

| Circuit | Gates | QC | Garbage | Depth |
|---|---|---|---|---|
| SR | 3 FG + 1 PG | 7 | 2 | 6 |
| JK | 2 FRG + 2 FG | 12 | 3 | 11 |

## V. NOISE EVALUATION

➢ *Noise Models and Setup*

Noise was modeled with quantum channels in the Kraus form of (13), where the operators satisfy $\sum E_i^\dagger E_i = I$ [15], [16]. Bit-flip noise with probability $p$ is given by (14), and depolarizing noise with probability $p$ by (15). Amplitude damping with decay parameter $\gamma$ has the operators of (16), written with matrix rows separated by semicolons, and phase damping with parameter $\lambda$ has the operators of (17).

$$\varepsilon(\rho) = \sum_i E_i \, \rho \, E_i^\dagger \tag{13}$$

$$\varepsilon(\rho) = (1 - p)\, \rho + p \, X\rho X \tag{14}$$

$$\varepsilon(\rho) = (1 - p)\, \rho + (p/3)(X\rho X + Y\rho Y + Z\rho Z) \tag{15}$$

$$E_0 = [1\ 0;\ 0\ \sqrt{(1-\gamma)}],\ E_1 = [0\ \sqrt{\gamma};\ 0\ 0] \tag{16}$$

$$E_0 = \sqrt{(1-\lambda)}\, I,\ E_1 = \sqrt{\lambda}\, |0\rangle\langle 0|,\ E_2 = \sqrt{\lambda}\, |1\rangle\langle 1| \tag{17}$$

Each channel was applied to every qubit that a gate acts on, immediately after that gate, so a CNOT is followed by one channel on each of its two qubits and a Toffoli gate by one on each of its three. The parameters were $p = \gamma = \lambda = 0.02$. Input preparation and measurement were noiseless. Counting every X, T, CNOT and Toffoli operation, the SR circuit has 10 operations that touch 16 qubit positions, and the JK circuit has 15 operations that touch 25. The simulations used Qiskit 2.6.1 with Aer 0.18.2, a fixed random seed, and 4096 shots for each of the eight inputs, which is 32 768 shots per circuit and noise model.

Two accuracies were computed from (18), where $N_{\text{correct}}$ counts the shots that reproduce the ideal result. The first requires the complete seven-bit register to match, including the garbage lines. The second requires only the two output bits, Q and Q′, to match. Because the accuracies are binomial proportions, 95% Wilson intervals [15] are used for uncertainty.

$$A = N_{\text{correct}} / N \tag{18}$$

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➢ *Results*

Table 5 gives the accuracies for all four noise models. Under ideal simulation both circuits were correct in every shot. The 95% intervals have half-widths of at most 0.5 percentage points, so differences of a point or more between entries are real.

Table 5 Accuracy Under Per-Gate Noise (0.02)

| Noise | SR full | JK full | SR Q, Q′ | JK Q, Q′ |
|---|---|---|---|---|
| Ideal | 100% | 100% | 100% | 100% |
| Bit-flip | 72.9% | 61.6% | 82.9% | 73.9% |
| Depolarizing | 85.0% | 77.9% | 90.8% | 85.1% |
| Amp. damping | 84.2% | 75.8% | 89.9% | 84.0% |
| Phase damping | 100% | 100% | 100% | 100% |

Under bit-flip noise the SR circuit kept 72.9% of its complete outputs and the JK circuit 61.6%. Depolarizing noise left 85.0% and 77.9%, and amplitude damping left 84.2% and 75.8%. Phase damping changed nothing. Counting only the output bits Q and Q′ raises every figure, but the order of the two circuits is the same. The results are plotted in Fig. 8.

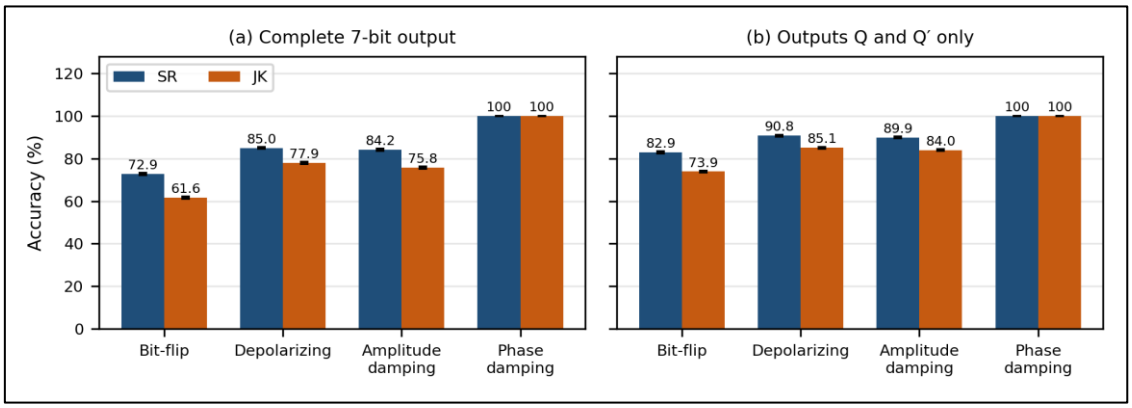



Fig 8 Accuracy of the SR and JK Circuits Under Per-Gate Noise, with 95% Wilson Intervals: (a) Complete Output Vector, (b) Outputs Q and Q′ Only.

## VI. DISCUSSIONS

Phase damping leaves both circuits untouched because every state in them is a computational-basis state, on which phase damping acts trivially. The 100% accuracy is therefore a property of the inputs rather than evidence of special robustness, and the circuits would behave differently on superposition inputs. All outputs are measured in the computational (Z) basis, and the prepared inputs are basis states with no coherence between $|0\rangle$ and $|1\rangle$. Phase damping only suppresses such off-diagonal terms, so it has nothing to act on here. No claim of general phase-error resistance is made.

The other three models separate the circuits clearly, and the separation follows circuit size. The JK circuit exposes 25 qubit positions to noise against 16 for the SR circuit. If each exposure flips its qubit independently with probability 0.02 and no flip is masked, the chance of a clean run is $0.98^n$, which is 72.4% for n = 16 and 60.3% for n = 25. The measured bit-flip accuracies of 72.9% and 61.6% sit just above these values, as expected when a few pairs of flips cancel. A smaller circuit is simply exposed to fewer errors.

Amplitude damping adds an input dependence that the other models do not have. It acts only on qubits holding 1, so inputs that put more qubits in the excited state lose more accuracy. Across the eight inputs the complete-output accuracy under amplitude damping ranged from 79.8% to 93.8% for the SR circuit and from 69.8% to 88.1% for the JK circuit, whereas under the other models the spread across inputs stayed below one percentage point. A noise study that tests only the all-zero input would miss this effect, which is why all eight inputs were used.

➢ *Comparison with the Reference Design*

Table 6 compares the circuits with the reference designs of [4], using the values reported there. The JK circuit lowers the quantum cost from 13 to 12, which is a reduction of 7.69% by (6), and its garbage count is unchanged. The SR circuit matches the reference cost of 7 and its two garbage outputs, so no saving is claimed for it. Depth was not reported for the reference designs, so only quantum cost, garbage outputs and delay can be compared. The saving in the JK circuit is small, and Section VI shows that the smaller SR circuit is the more noise-tolerant of the two, so cost and noise exposure have to be weighed together when a design is chosen.

Table 6 Comparison with the Reference Design [4]

| Design | Quantum Cost | Garbage Outputs | Delay (Δ) | Circuit Depth | Qiskit Noise Evaluation |
|---|---|---|---|---|---|
| Reference SR [4] | 7 | 2 | 7 | Not reported | Not established in comparison |
| Reference JK [4] | 13 | 3 | 13 | Not reported | Not established in comparison |

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| | | | | | |
|---|---|---|---|---|---|
| Proposed SR | 7 | 2 | 7 | 6 | Included |
| Proposed JK | 12 | 3 | 12 | 11 | Included |

## VII. CONCLUSION

Reversible SR and JK flip-flop circuits were built from Feynman, Peres and Fredkin gates, implemented in Qiskit, and verified against their characteristic equations for all eight combinations of present state and inputs. The SR circuit has quantum cost 7, two garbage outputs and depth 6. The JK circuit has quantum cost 12, three garbage outputs and depth 11, which is a 7.69% saving over the reference cost of 13. Under noise applied after every gate, the SR circuit held its complete output vector in 73% to 85% of shots and the JK circuit in 62% to 78%, depending on the model, while phase damping had no effect on basis-state inputs. The difference between the circuits tracks the number of noisy gate operations, so the cost saving of the JK design does not make it more noise-tolerant.

The study has limits. The circuits compute the state-update function, with the present state supplied as an input, and clocking and master–slave structure are not modeled. The noise models are simple, with the same error probability on every gate, and no run on physical quantum hardware was made. Future work should add clocked master–slave versions, noise models calibrated to a real device, and execution on IBM Quantum hardware, so that the simulated trends can be compared with measured ones.

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