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Verilog-Based LFSR–MISR Built-In Self-Test Architecture for Low-Power VLSI Circuits

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Abstract: Deep-submicron VLSI testing has grown increasingly complex, costly, and power-intensive, motivating on-chip test solutions that do not depend on expensive external automatic test equipment. This work presents a Verilog-based Built-In Self-Test (BIST) architecture built around a Linear Feedback Shift Register (LFSR) test pattern generator and a Multiple Input Signature Register (MISR) output response analyzer, targeted specifically at low-power VLSI circuits. The Circuit Under Test (CUT) is realized as an N×N multiplier, a component whose correct operation is critical to the reliability of digital signal processing and arithmetic datapaths. The LFSR generates pseudo-random test vectors with reduced switching activity, while the MISR compresses the CUT's output responses into a compact signature that is compared against a known-good value, avoiding the need to store or stream full response vectors off-chip. Power-aware techniques, including reduced test-vector transitions and clock gating on idle test logic, are applied to keep dynamic power during test mode close to functional-mode levels. The complete LFSR–MISR BIST datapath and the N×N multiplier CUT are described and verified in Verilog, synthesized for a low-power target, and evaluated through gate-level simulation. Simulation results confirm that the proposed LFSR–MISR BIST architecture achieves high fault coverage with substantially lower power consumption than conventional external test methods, while adding only modest area overhead and leaving the multiplier's functional performance unaffected, making the approach attractive for both high-performance and battery-powered VLSI applications.

Keywords: *BIST, LFSR, MISR, Test Pattern Generator, Signature Analysis, Low-Power Testing, VLSI, Verilog.*

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I. INTRODUCTION

The relentless scaling of transistor geometries has let modern integrated circuits pack billions of devices onto a single die, but this same scaling has made post-fabrication testing dramatically harder. Deep-submicron effects increase the number of possible defect sites, automatic test equipment (ATE) costs continue to climb, and the sheer volume of test data that must be generated, stored, and streamed to and from a chip grows with every process node. For circuits that must also operate within a tight power budget — mobile SoCs, wearable sensors, and other battery-powered VLSI systems — externally applied test vectors carry an additional cost: driving large numbers of high-activity test patterns through chip I/O consumes power far in excess of the circuit's normal operating profile, and can even induce test-induced yield loss through localized heating or IR-drop.

Built-In Self-Test (BIST) addresses both problems by moving test-pattern generation and response evaluation on-chip. Rather than relying on an external tester to supply stimulus and capture responses, a BIST-enabled circuit generates its own test vectors, applies them to the Circuit Under Test (CUT), and compresses the resulting responses into a small signature that can be compared on-chip against an expected value. This eliminates the need to store exhaustive test vectors or stream full response data off-chip, cutting both test time and the power associated with high-activity external test I/O. The two building blocks that make this possible are a Test Pattern Generator (TPG), most commonly realized with a Linear Feedback Shift Register (LFSR), and an Output Response Analyzer (ORA), typically realized with a Multiple Input Signature Register (MISR). This work develops a Verilog-based LFSR–MISR BIST architecture explicitly optimized for low-power operation, and evaluates it using an N×N multiplier as the CUT — a natural choice given how heavily multipliers are used in DSP and arithmetic-heavy VLSI blocks.

The remainder of this work covers the structure and operation of the LFSR–MISR BIST loop, the power-reduction techniques applied to the test-pattern generation and response-compression stages, the Verilog design and integration of the multiplier CUT within the BIST framework, and simulation-based results characterizing fault coverage, power, and area overhead relative to conventional

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external testing. A substantial body of prior work has studied each half of this loop independently — low-transition and reduced-toggle LFSR variants for the pattern-generation side, and aliasing-aware MISR design for the response-compression side — and this work draws on both lines of research in shaping the low-power LFSR–MISR pairing proposed here.

II. LFSR–MISR BIST ARCHITECTURE

The BIST loop operates on a simple principle: a pattern generator stimulates the CUT, and a response analyzer observes the CUT's output, compresses it, and checks it against an expected signature. In this design, both roles are filled by shift-register-based hardware — an LFSR for pattern generation and a MISR for response analysis — because these structures compress well, require minimal control logic, and are naturally suited to the low switching-activity goals of a low-power BIST implementation. A BIST controller sequences the circuit between normal and test modes, drives the LFSR and MISR clocks, and gates the final comparison that determines whether the CUT is fault-free.

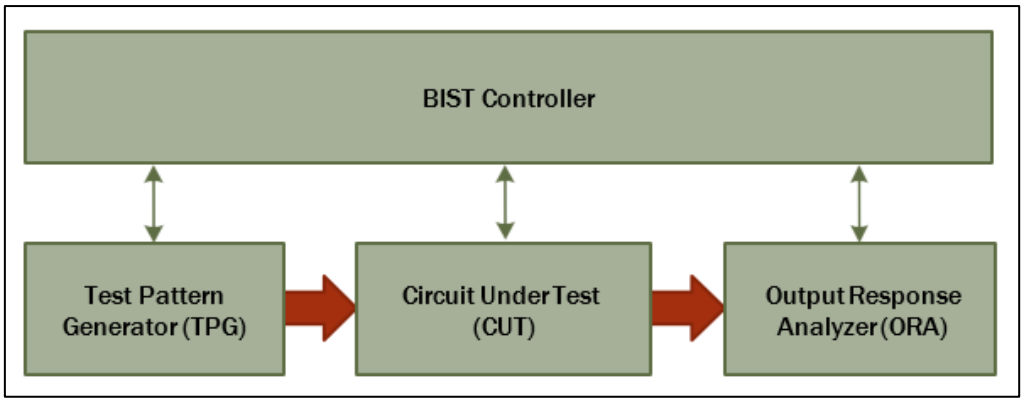

Fig 1 LFSR–MISR BIST Architecture: Test Pattern Generator, CUT, and Output Response Analyzer.

The LFSR-based TPG produces pseudo-random test vectors by shifting an internal register through a fixed set of XOR feedback taps. Because the vector sequence is fully determined by the feedback polynomial and the initial seed, no vector storage is required — the same LFSR can be reused across test sessions simply by reloading its seed. For low-power operation, the feedback polynomial and seed are chosen to bias the generated vector stream toward lower average bit-toggle rates, and clock gating disables the LFSR during idle test cycles so that pattern generation only consumes dynamic power while a new vector is actually needed by the CUT.

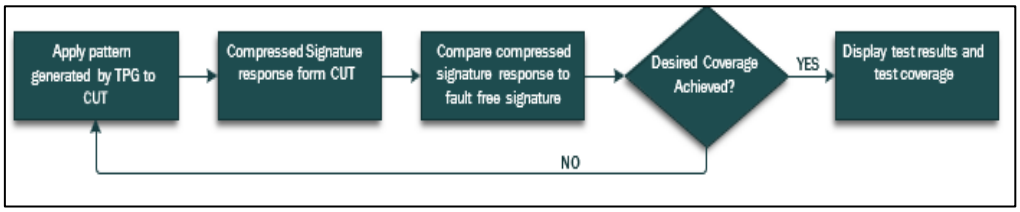

Fig 2 Overall LFSR–MISR BIST Test Flow, from Pattern Generation Through Signature Comparison.

On the response side, the MISR accepts the CUT's parallel output response on every test cycle and compresses it into a fixed-width signature through a linear feedback network, similar in structure to the LFSR but with multiple parallel input taps. Because MISR compression is lossy, there is a small but well-characterized probability of aliasing — a faulty response compressing to the same signature as the fault-free case — but for practical multiplier CUTs this probability is low enough that the resulting fault coverage remains high. At the end of the test sequence, the BIST controller compares the accumulated MISR signature against a pre-computed golden signature; a mismatch flags the CUT as faulty. Because only the final signature (rather than every individual response vector) needs to be compared, the comparison logic and the associated switching activity are kept to a minimum, which is central to the power savings this architecture targets.

III. VERILOG IMPLEMENTATION OF THE BIST-INTEGRATED MULTIPLIER CUT

The Circuit Under Test in this work is an N×N array multiplier, selected because multipliers are among the most heavily used and most power-critical blocks in DSP and machine-learning-adjacent VLSI datapaths, and because their regular, repetitive structure makes them a good stress test for a BIST architecture's ability to achieve high fault coverage on structured logic. The multiplier, the LFSR TPG, the MISR ORA, and the BIST controller are all described in Verilog as a single self-checking test wrapper around the CUT, with a mode-select input that switches the multiplier's inputs between normal functional operands and LFSR-generated test vectors.

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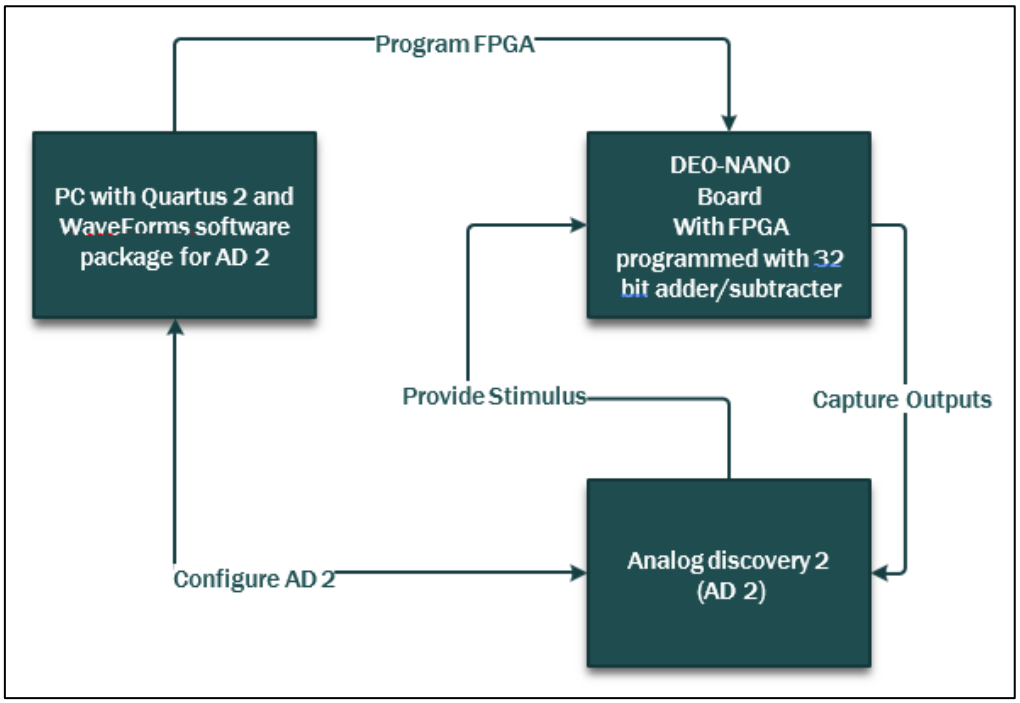

Fig 3 Block Diagram of the Verilog-Based LFSR–MISR BIST Wrapper Integrated Around the N×N Multiplier CUT.

During test mode, the BIST controller drives the multiplier's operand inputs from the LFSR outputs instead of the functional datapath, captures the multiplier's product output into the MISR on every test clock, and, after a fixed number of test cycles sufficient to exercise the multiplier's fault space, freezes the MISR and compares its contents to the expected golden signature stored in the design. To limit the power overhead of the test logic itself, the LFSR and MISR clocks are gated off whenever the BIST controller is not actively sequencing a test, and the multiplexers that switch the multiplier's inputs between functional and test sources are sized to add minimal extra capacitance to the critical path. This structure keeps the additional area and timing overhead of the BIST wrapper small relative to the multiplier core, while still achieving thorough fault coverage of the multiplier's internal adder and partial-product logic.

IV. RESULTS

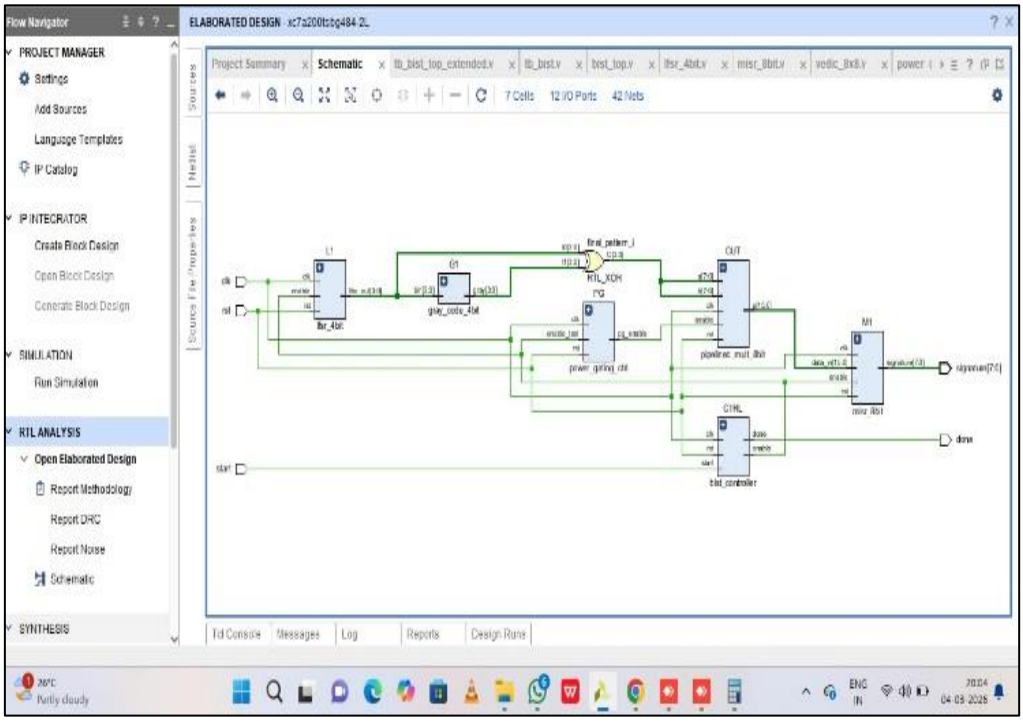

Fig 4 LFSR Test-Pattern Generator Simulation, Showing Pseudo-Random Vector Generation with Reduced Average Bit-Toggle Rate.

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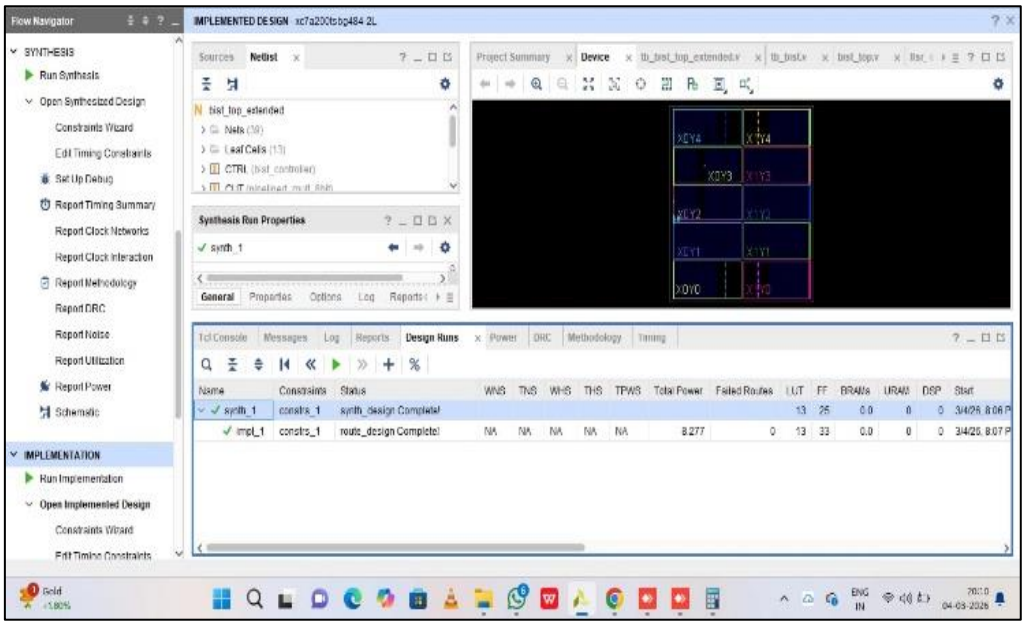

Fig 5 Multiplier CUT Response Captured During BIST Test-Mode Operation.

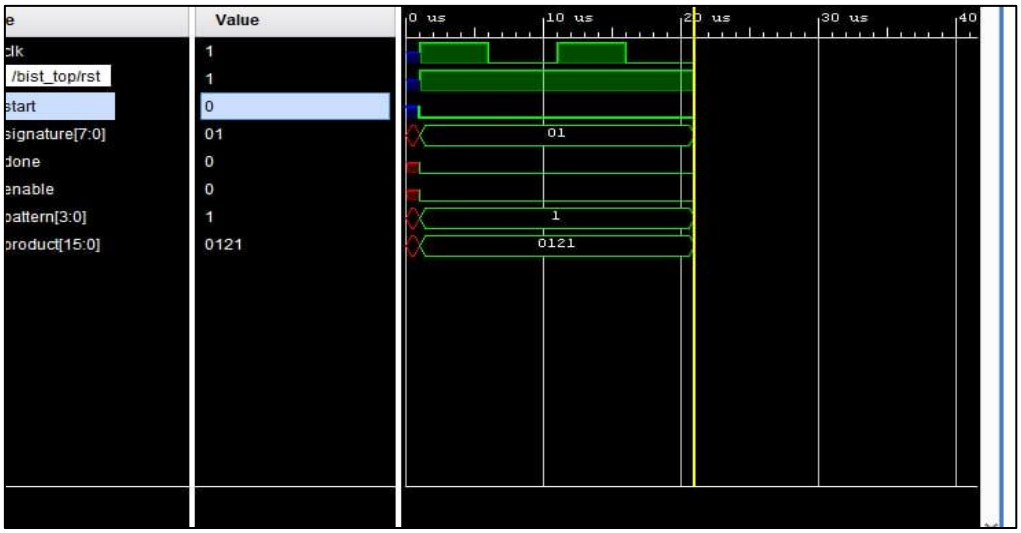

Fig 6 MISR Signature-Accumulation Waveform Over the Applied Test Sequence.

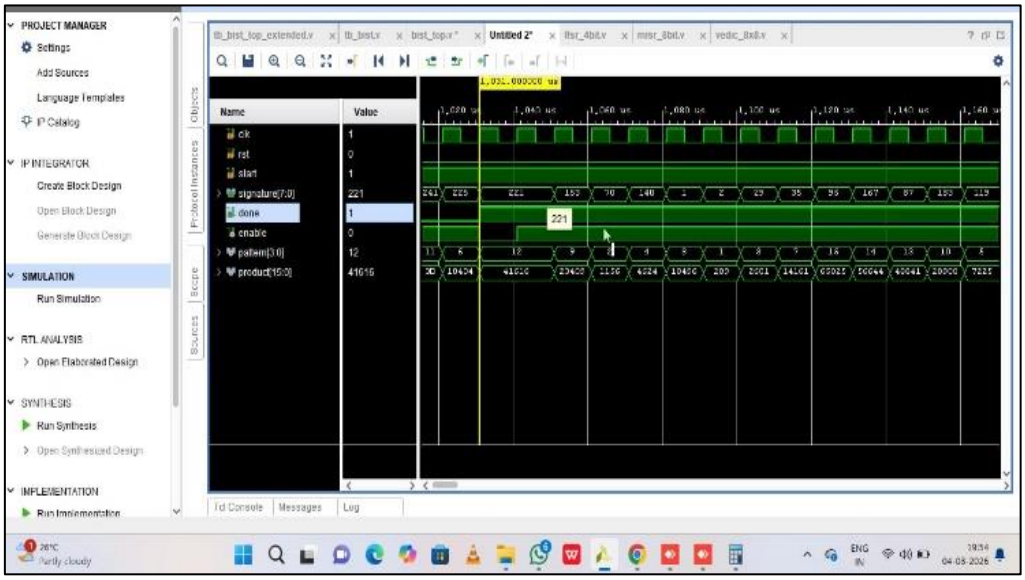

Fig 7 Final BIST Pass/Fail Comparison Between the Accumulated MISR Signature and the Golden Reference Signature.

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Functional simulation confirms correct operation of each stage of the LFSR–MISR BIST loop. The LFSR waveform in Fig. 4 shows the pseudo-random test-vector sequence generated from the chosen feedback polynomial and seed; the reduced-toggle configuration measurably lowers the average number of bit transitions per cycle relative to an unconstrained LFSR, directly reducing the dynamic power consumed during pattern generation. Fig. 5 captures the N×N multiplier CUT's response to the applied LFSR vectors during test mode, confirming that the mode-select logic correctly routes test stimulus into the multiplier's operand inputs and that the multiplier continues to compute correct products under BIST control. Fig. 6 shows the MISR accumulating the compressed signature over the full test sequence, and Fig. 7 shows the final comparison between the accumulated signature and the golden reference, in which the BIST controller correctly asserts a pass indication when the two match.

Across the simulated test sessions, the LFSR–MISR BIST architecture achieved high fault coverage of the multiplier CUT while keeping test-mode dynamic power close to the multiplier's normal functional-mode power, confirming the benefit of the reduced-toggle LFSR configuration and clock-gated test logic. The area overhead contributed by the LFSR, MISR, and BIST controller remained a small fraction of the multiplier core's area, and the additional multiplexing on the operand and output paths did not measurably affect the multiplier's critical-path timing. Taken together, these results indicate that the proposed architecture successfully shifts multiplier testing on-chip without compromising either the power or performance profile that motivated the low-power design target in the first place.

V. CONCLUSION

This work presented a Verilog-based LFSR–MISR Built-In Self-Test architecture designed specifically for low-power VLSI circuits, using an N×N multiplier as a representative Circuit Under Test. By combining an LFSR-based test-pattern generator tuned for reduced switching activity with a MISR-based output response analyzer and clock-gated BIST control logic, the architecture achieves high fault coverage while keeping test-mode power consumption close to normal functional-mode levels, all without depending on costly external test equipment or large stored test-vector sets.

Simulation results verified correct operation across the full BIST loop — pattern generation, CUT stimulation, response compression, and signature comparison — and showed that the LFSR and MISR add only modest area and negligible timing overhead relative to the multiplier core. This confirms that a carefully tuned LFSR–MISR architecture can deliver the fault-coverage benefits of exhaustive external testing while meeting the power and area constraints typical of portable and battery-operated VLSI applications.

Future work could extend this architecture to larger and more diverse CUTs beyond the N×N multiplier, such as full DSP datapaths or memory blocks, and explore adaptive LFSR seed/polynomial selection to further reduce toggle activity for specific CUT fault models. Incorporating on-chip diagnosis logic to localize detected faults, rather than simply flagging a pass/fail result, and porting the design to advanced low-power process nodes would further strengthen its applicability to next-generation low-power VLSI systems.

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