Volume 10, Issue 1, January – 2025 International Journal of Innovative Science and Research Technology
ISSN No:-2456-2165 https://doi.org/10.5281/zenodo.14651164

FIFO Implementation in Manufacturing: Streamlining Production Processes Minimizing Work-in-Progress Inventory

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Abstract:- This is a template and guidelines for, First In, First Out (FIFO) inventory management technique within manufac-turing settings based on its potential of making production more efficient and with minimal work-in-progress (WIP) inventories. It delves deeper into the theoretical framework that explains FIFO through its concepts and benefits against other inventory management systems. Further, it addresses actual case studies and empirical evidence to validate practical outcomes of imple-menting FIFO in varied manufacturing contexts. [6] The paper elaborates further on how FIFO permits free flow of materials since the oldest inventory is acquired first, thus preventing obsolescence and waste build-up. Further, it establishes that it ensures optimal levels of inventory so that overproduction and excess build up of inventory is avoided. Through synthesis of existing literature and industry insights, the research delivers an explanation regarding the mechanisms by which FIFO improves production efficiency and reduces cycle times.

Keywords:- *ASIC Design Flow, Artificial Intelligence (AI),Floor Planning, Internet of Things(IoT), Partitioning Simplified Cir-cuits, Physical Designing, RTL Design.*

I. INTRODUCTION

The bottom line of manufacturing remains efficiency and low cost. Such companies are always looking for strategies which help to optimize the production process as much as possible with least waste and better productivity. So, the strategy of inventory management becomes an integral part of these goals because it influences the material movement through the production process [2]. Among the inventory management methods applied, the most commonly used one that helps streamline the production process while reducing WIP inventories is the FIFO approach. FIFO is the principle where old inventory is consumed or sold before new inventory, meaning that goods must be consumed in the order received. Even though FIFO has been considered one of the funda-mental principles of inventory management for decades, its application within manufacturing environments has recently received growing attention. It is more clearly evident today with companies striving to optimize their supply chains, reduce holding costs, and generally operate more efficiently. The implementation of FIFO in manufacturing involves the strate-gic reevaluation of inventory control practices, production scheduling, and material flow management. Manufacturers have several key objectives by following the FIFO principle: they minimize obsolescence through the use of older inventory items before newer items, reduce excess inventory carrying costs, and keep overall production efficient with a smooth material flow.

II. LITERATURE SURVEY

The use of First In, First Out (FIFO) inventory management in manufacturing has always been of great interest to both researchers and practitioners. This literature review will discuss existing studies and insights about the implementation of FIFO in a manufacturing environment with an emphasis on how it streamlines the production process and minimizes WIP inventories. [13]

- *Theoretical Background:*

Research works in the area of FIFO in inventory management have deeply covered its theoretical foundation. In this study we established the economics with which FIFO operates. To explain, we presented ways in which FIFO ensures cost consis-tency and minimizes holding costs. Based on this foundation, current researchers have further analyzed how the adoption of FIFO procedures would significantly impact the manufacturing operations. [15]

- *Benefits of FIFO Implementation:*

Numerous studies have highlighted the benefits of implement-ing FIFO in manufacturing settings have been demonstrating that FIFO leads to lower holding costs and reduced risk of inventory obsolescence. Similarly,this research [5], empha-sized the positive impact of FIFO on production efficiency, citing improved material flow and reduced cycle times as key advantages.

- *Practical Applications and Case Studies:*

Empirical research and case studies have provided valuable insights into the practical implications of FIFO implementa-tion in manufacturing [12] demonstrating its effectiveness in reducing WIP inventories and improving overall operational efficiency.

- *Challenges and Considerations:*

Despite the benefits, the implementation of FIFO in manu-facturing is not problem-free. Some factors that hinder the effective implementation of FIFO practices have been

ISSN No:-2456-2165 https://doi.org/10.5281/zenodo.14651164

found by researchers to include logistical complexities, cultural re-sistance, and technological limitation,identified some of the main challenges manufacturers face in implementing FIFO as problems with inventory tracking and coordination.

There are many ways in which the future work and practical advice to manufacturers wanting to implement FIFO in their operations. [11] These include the development of advanced inventory management systems, the integration of emerging technologies such as Internet of Things (IoT) and Artificial Intelligence (AI), and the implementation of robust change management strategies. Additionally, there is a need for further empirical research to assess the long-term impacts of FIFO implementation on manufacturing performance and competi-tiveness.

III. METHODOLOGY

This thesis aims to implement the RTL to GDSII flow for a FIFO system core. The design process employs a 45nm technology library, including slow.lib and fast.lib files, a library exchange file (.lef), Synopsys design constraints (.sdc) file, and various scripts for synthesis, static timing analysis, and physical design. [9] In the frontend phase, the functionality of the RISC-V processor was verified using the NC Launch simulator tool by Cadence.

Following verification, the Cadence Genus tool generate's the gate-level netlist. The backend physical design was carried out with the Cadence Innovus tool, involving steps like floor-planning, partitioning, placement, and routing. Partitioning simplified complex circuits, floorplanning assigned boundaries to all blocks, placement arranged standard cells in the core area, and routing established connections according to the netlist. [3]. Performance was analysed and optimised in both pre-CTS and post-CTS stages. This work encompasses both the frontend and backend aspects of the RTL to GDSII flow, as shown in Figure 1.

A. Simulation

The simulation is carried in the Xcelium, Xcelium is the engine that performs the actual simulation, while NCLaunch provides the front-end interface for user interaction and control. Required files are: Register Transfer Level (RTL) code: This is the high-level description of the circuit's behaviour, written in a hardware description language (HDL) like Verilog or VHDL. [7] Testbench: This is a separate HDL file that generates input signals and checks the output responses of the design under test (DUT). It simulates the environment in which the DUT will operate. The typical simulation flow involves the following steps: • Compilation:The RTL design and testbench are compiled into an executable simulation model. • Elaboration:The simulation model is linked with the standard cell libraries and technology libraries. • Simulation: The testbench generates stimuli, the DUT responds, and the outputs are compared with expected results. • Debugging: If errors or violations are detected, the design is debugged and modified. • Regression: The simulation is repeated with different testbenches to ensure the design's robustness under various scenarios.

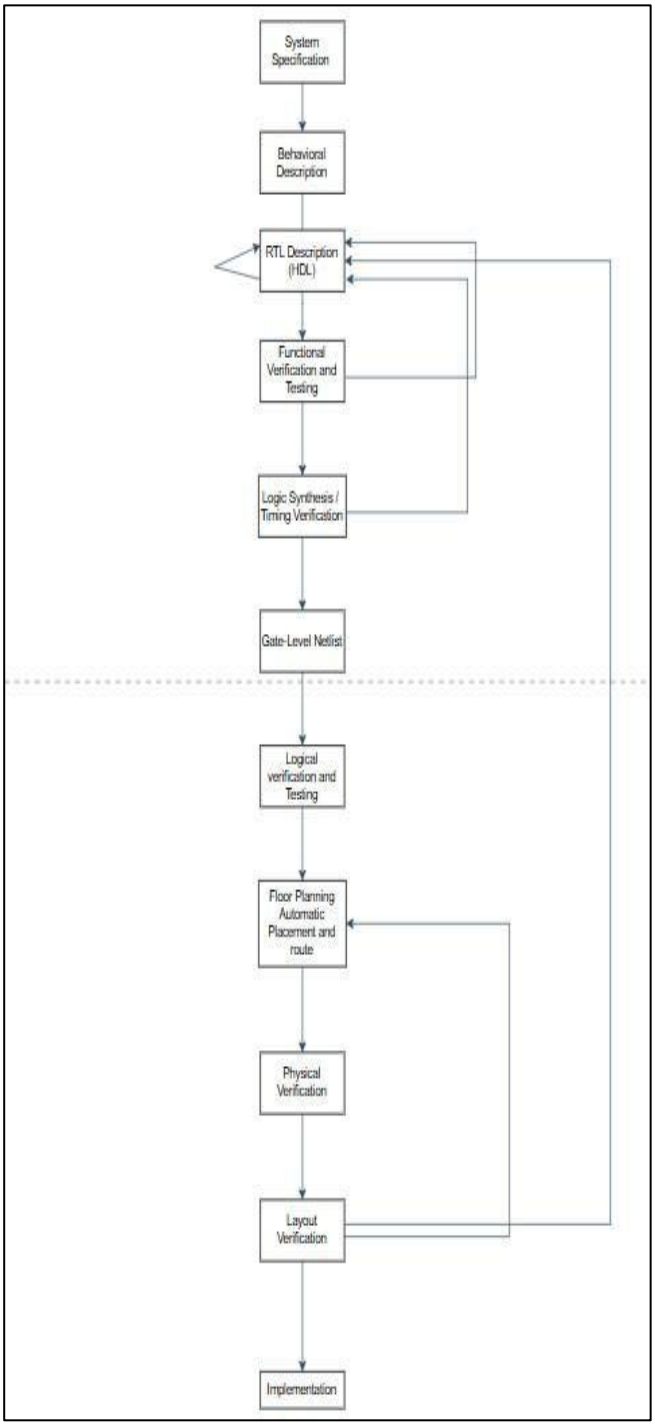

Fig 1 ASIC Design Flow

B. Synthesis

The synthesis process, executed using the Genus tool, transforms the register transfer logic (RTL) design into a gate level netlist. This transformation requires RTL code, Synopsys Design Constraints (SDC) file, and a TCL script to automate the entire flow. The resulting gate-level netlist, along with a modified SDC file, serves as input to the physical design process. [1].Additionally, the synthesis tool generates reports on timing, area, and power to evaluate the design's performance at the gate level.

ISSN No:-2456-2165 https://doi.org/10.5281/zenodo.14651164

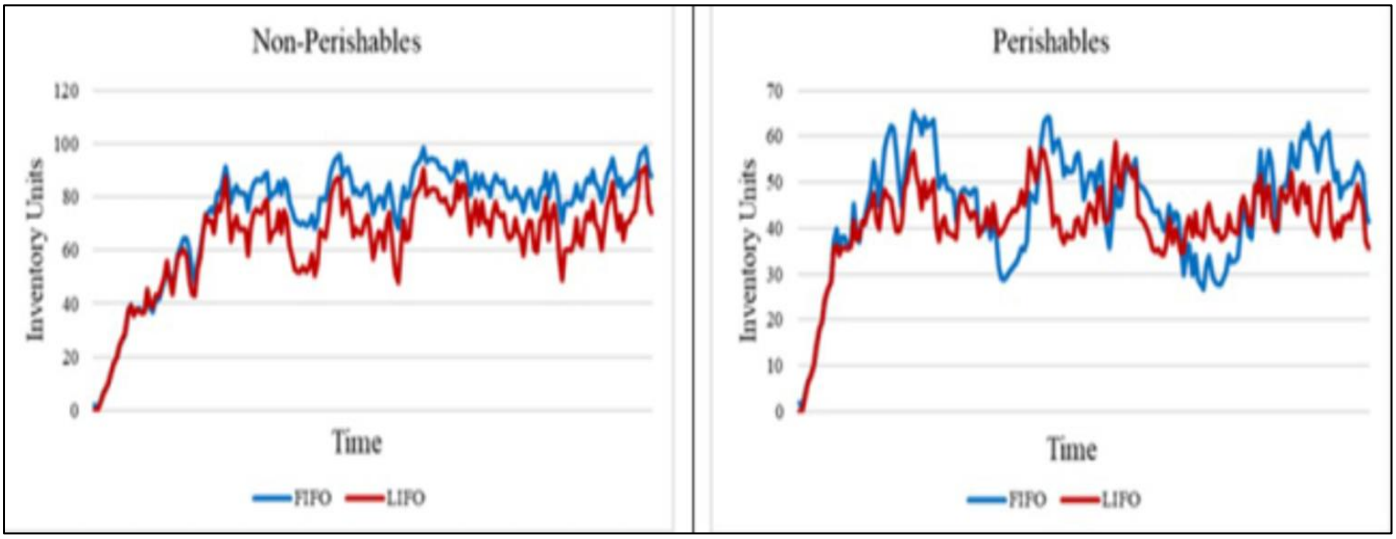

Fig 2 Aggregate Comparison Table of FIFO and LIFO

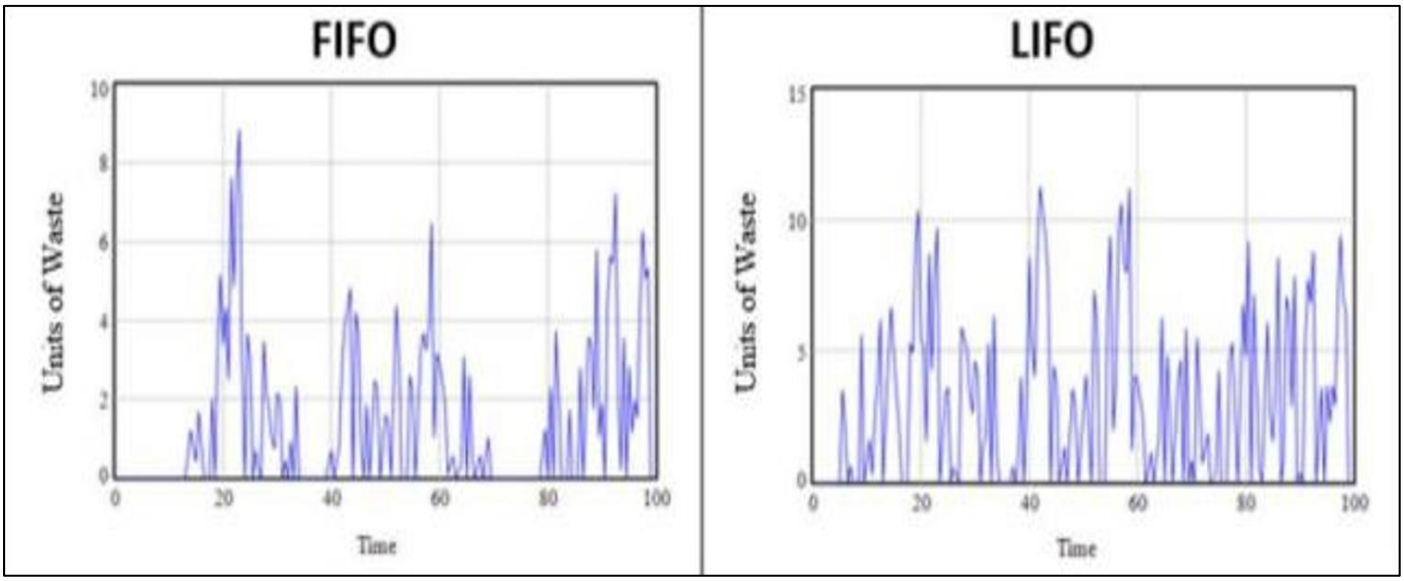

Fig 3 Sales Comparison Table of FIFO and LIFO

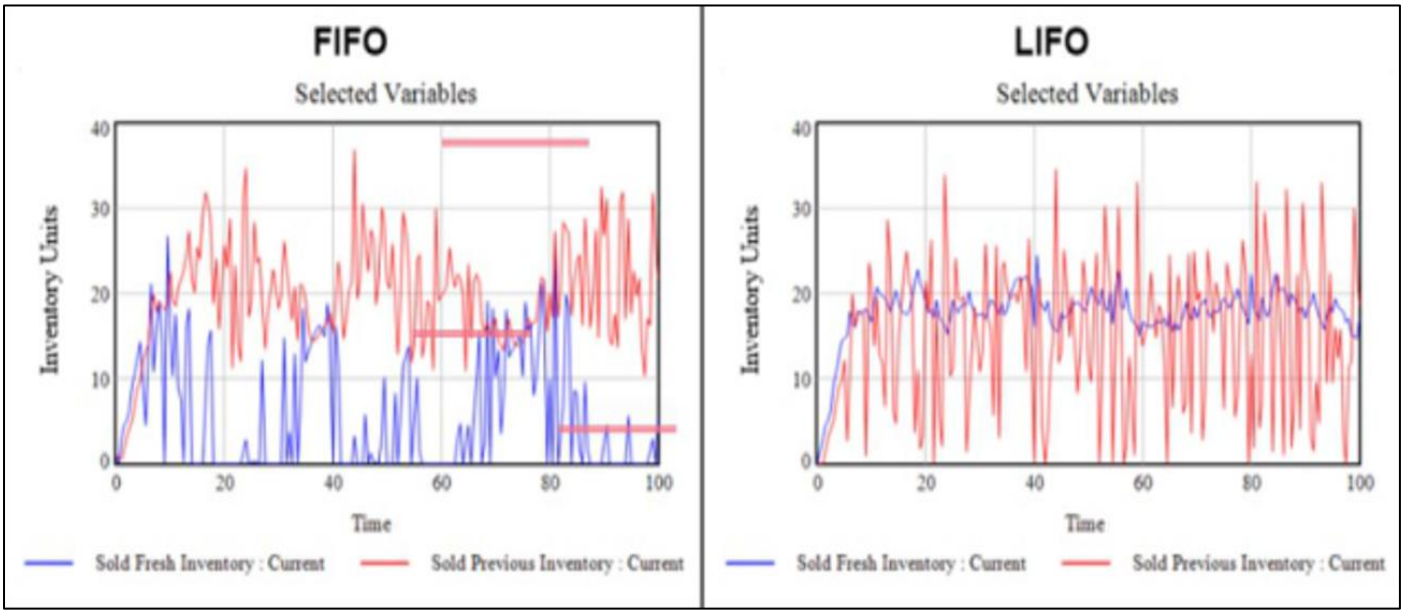

Fig 4 Sales Comparison Table of FIFO and LIFO

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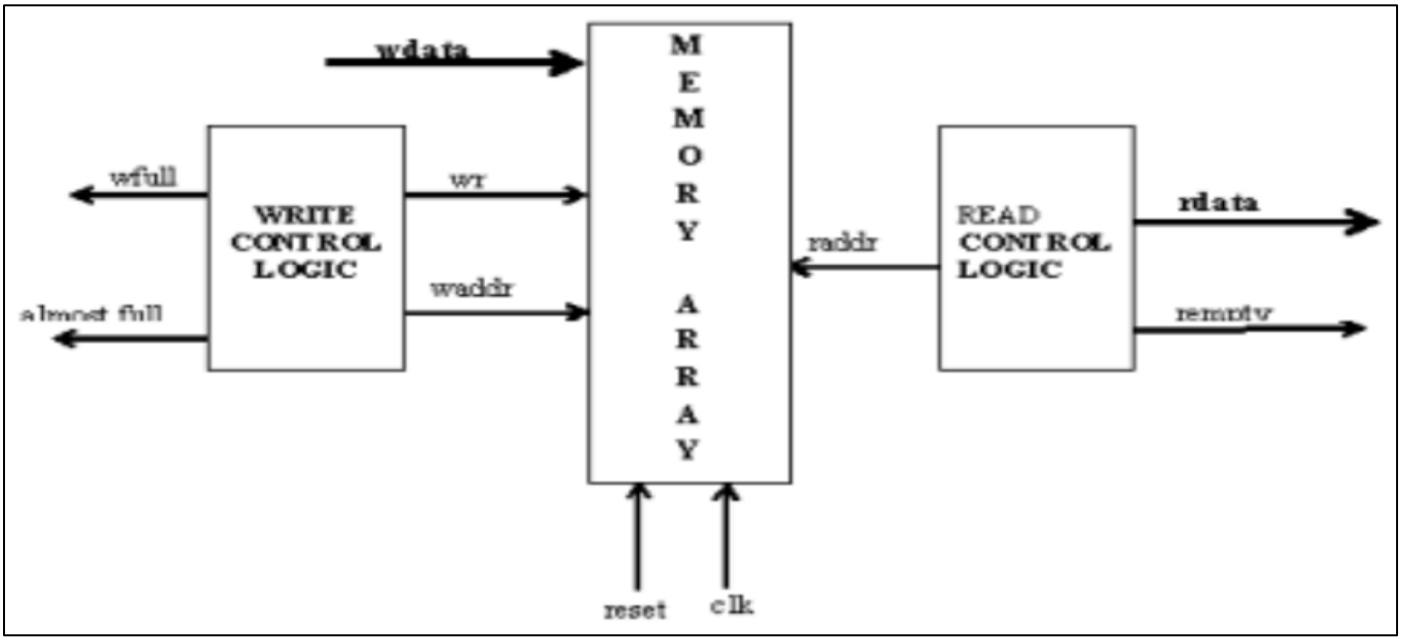

Fig 5 Block Diagram of FIFO

C. Physical Design

The Cadence Innovus tool provides the physical design process, with gate-level placement and routing of a Verilog netlist. The Innovus places standard cells, performs power routing, and produces comprehensive reports on timing, area, power, and design rule checks. All the above inputs go into this flow, including gate-level netlist, technology library files (.lib and.lef), Synopsys Design Constraints (SDC) from synthesis tool Genus, and the TCL script used to start up the design load-up. The process has optimization in both pre and post-CTS steps, for which reports come at each of the steps along with timing, area, and power metrics. The final GDSII file is generated for the FIFO processor, which is a standard format for integrated circuit layout data, upon completion of post-layout STA. [6]

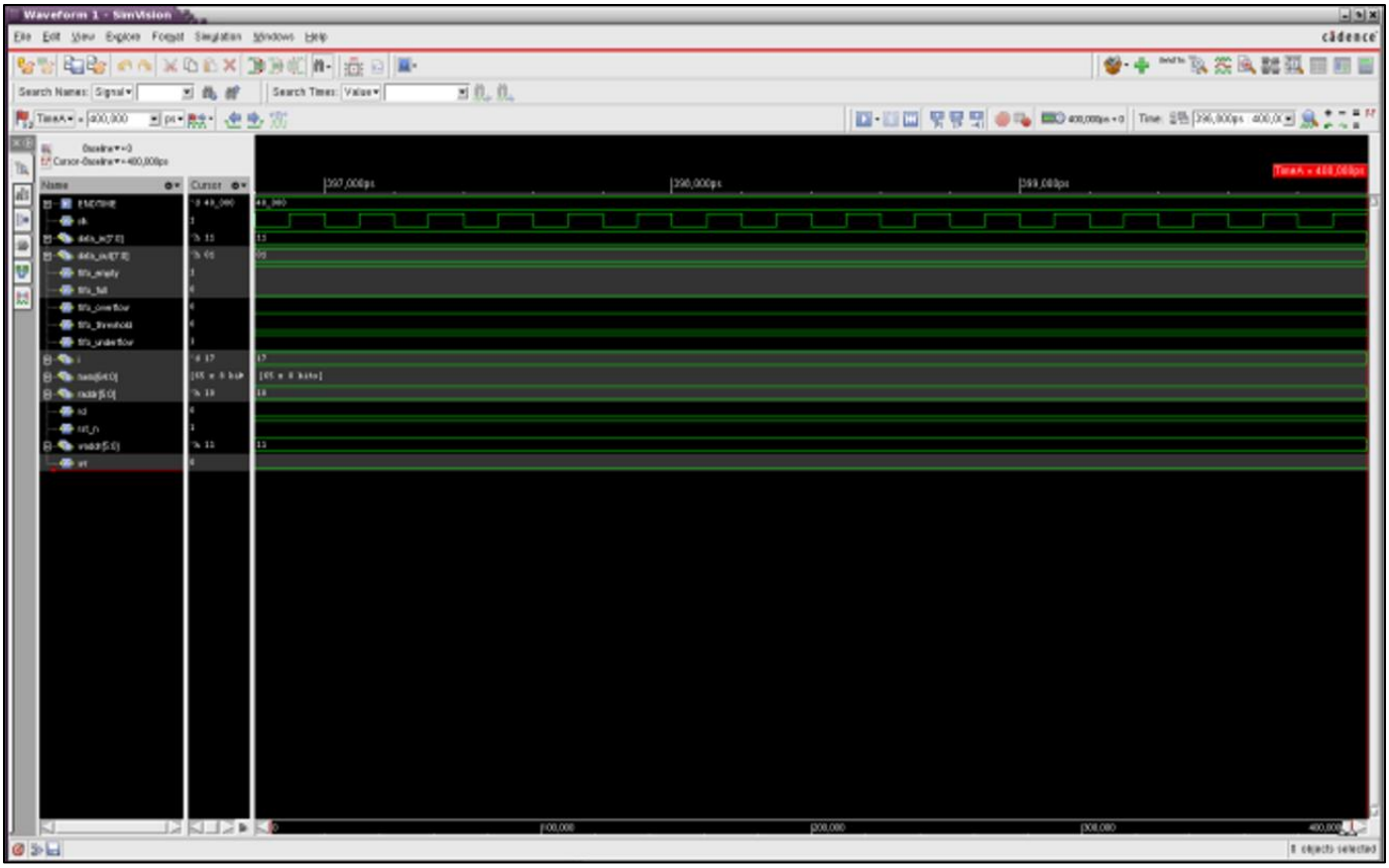

Fig 6 Simulation Diagram

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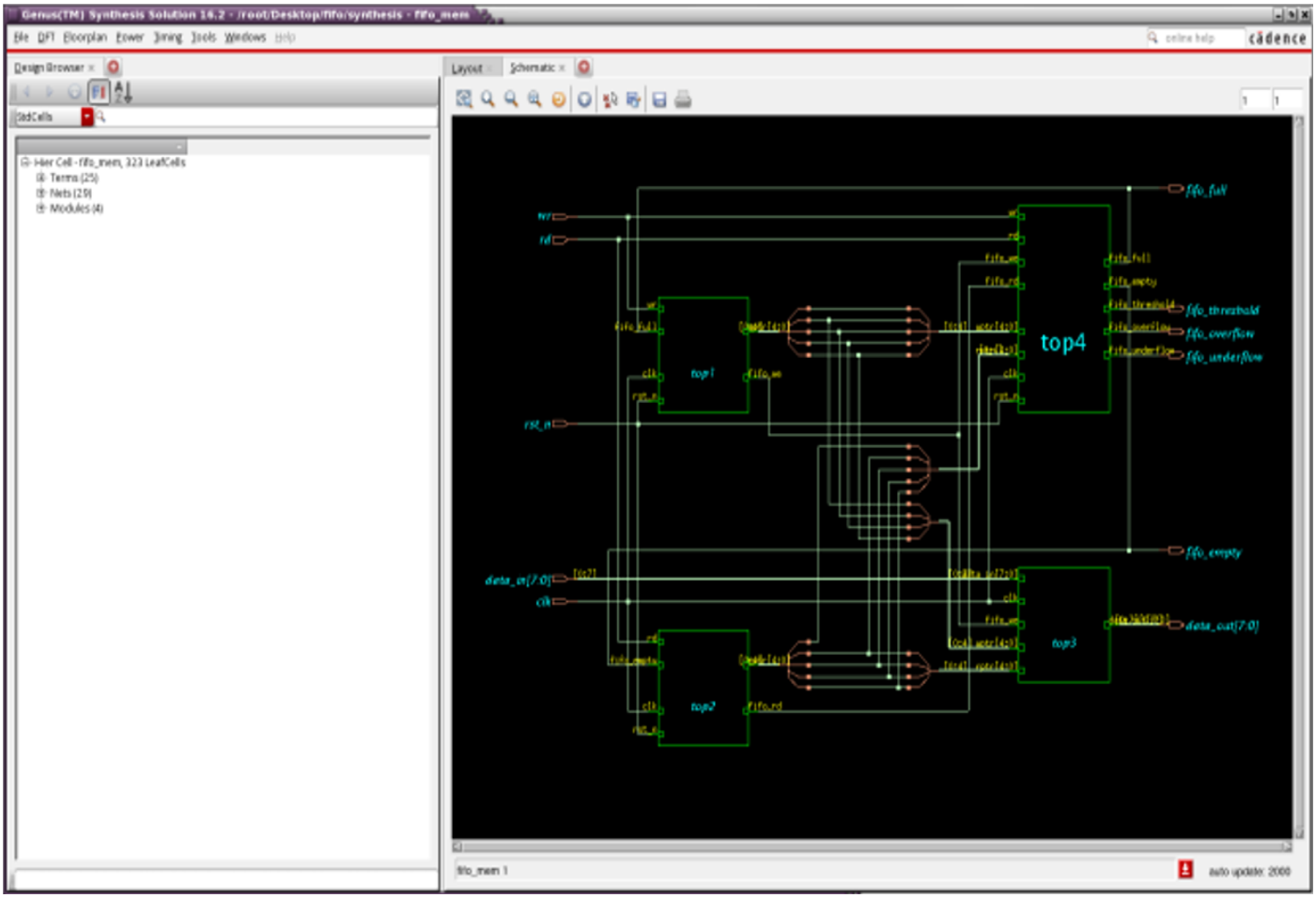

Fig 7 Synthesis diagram

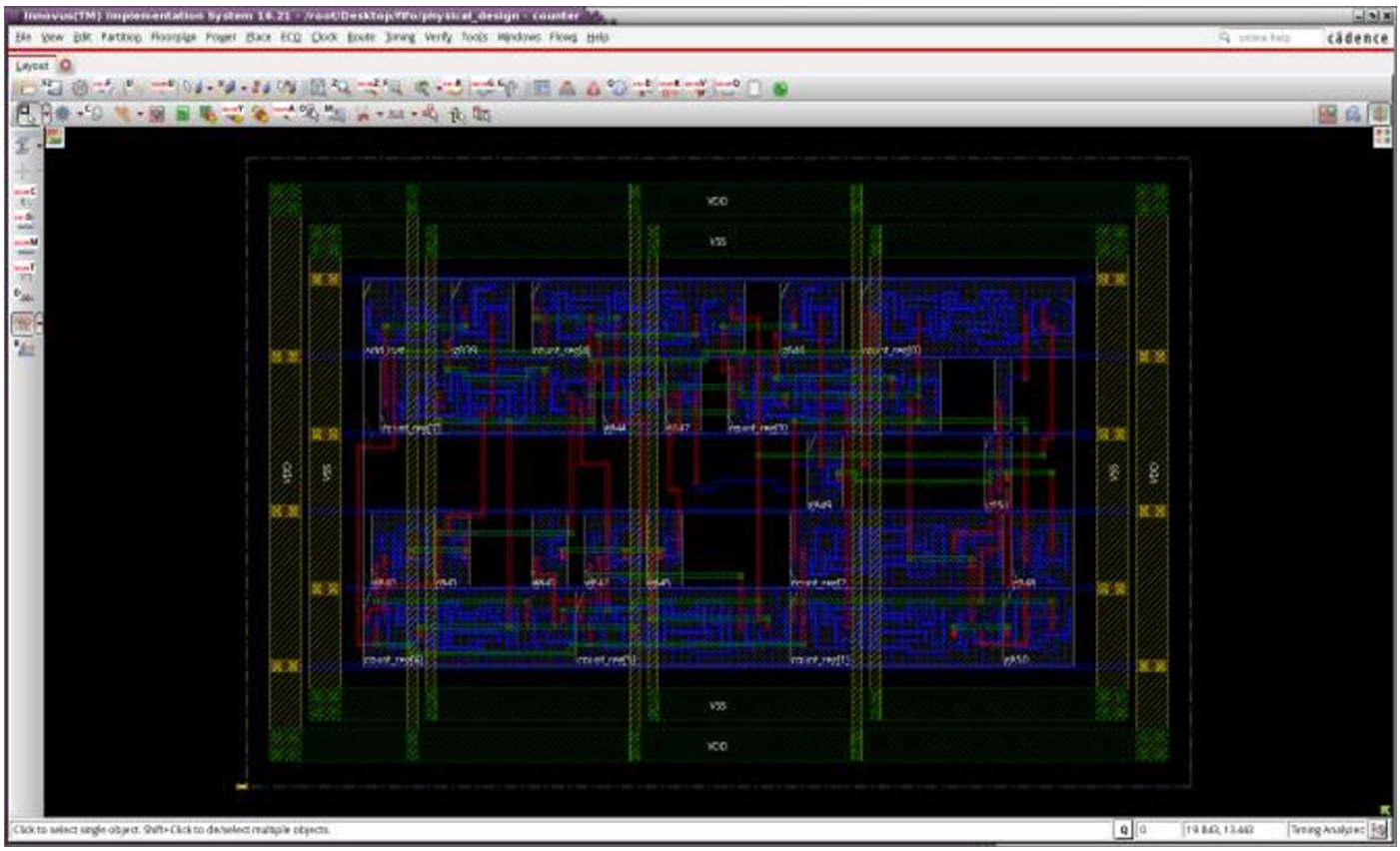

Fig 8 Physical Design

ISSN No:-2456-2165 https://doi.org/10.5281/zenodo.14651164

Table 1 Comparative Analysis

Timing	Power	Observed Timing	Referred Timing	Observed Power	Referred Power
Minimum Period	Total Internal Power	6.809 ns	4.907 ns	0.04 W	0.03 W
Minimum Input Period before Arrival Clock Time	Total Switching Power	7.537 ns	8.134 ns	0.005 W	0.004 W
Minimum Output Required time after Clock	Total Leakage Power	4.620 ns	6.874 ns	0.000002 W	0.000031 W
Speed Grade	Total Power	-4	-4	0.00517 W	0.00638 W

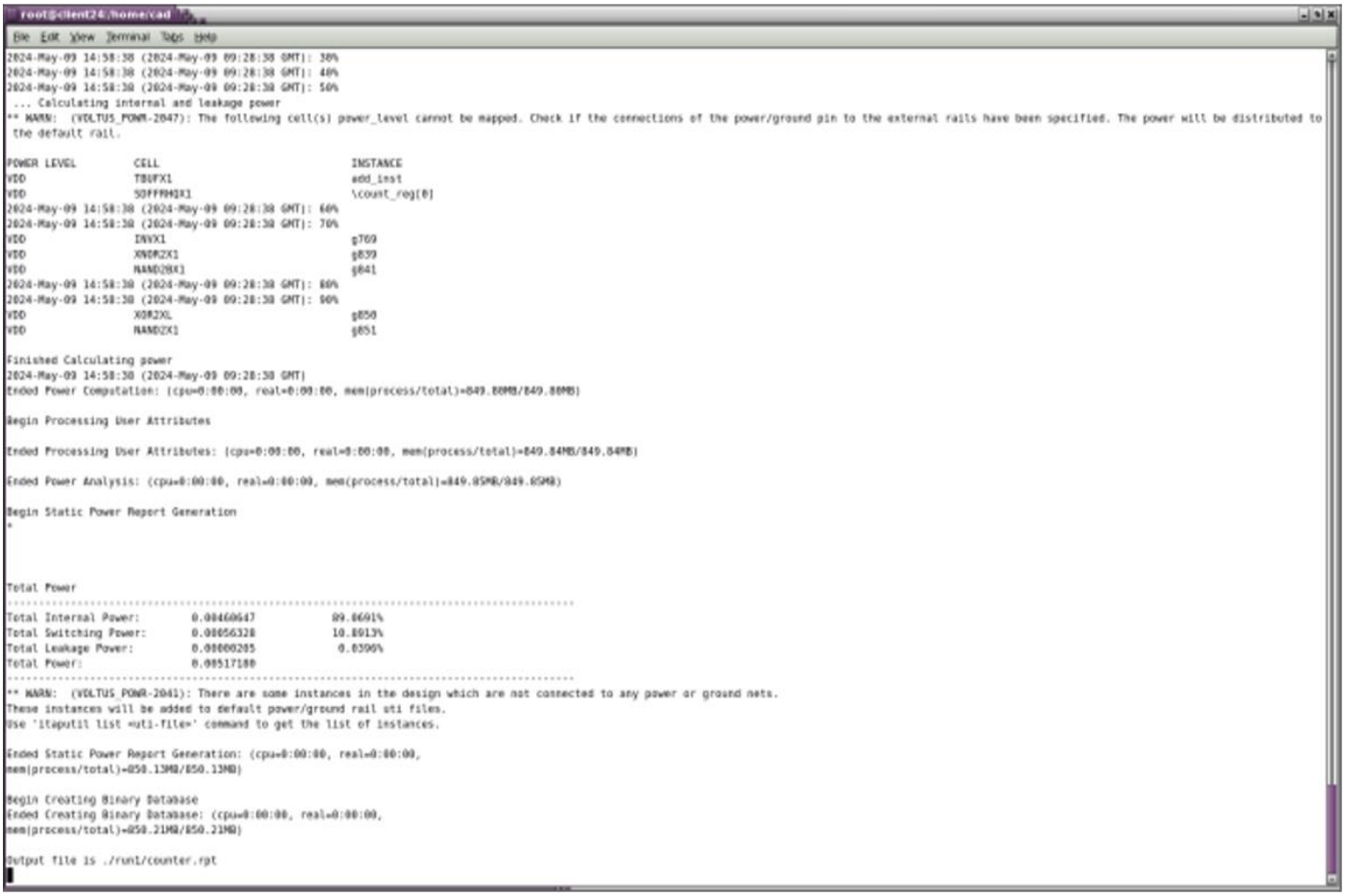

Fig 9 Results of the Experiment

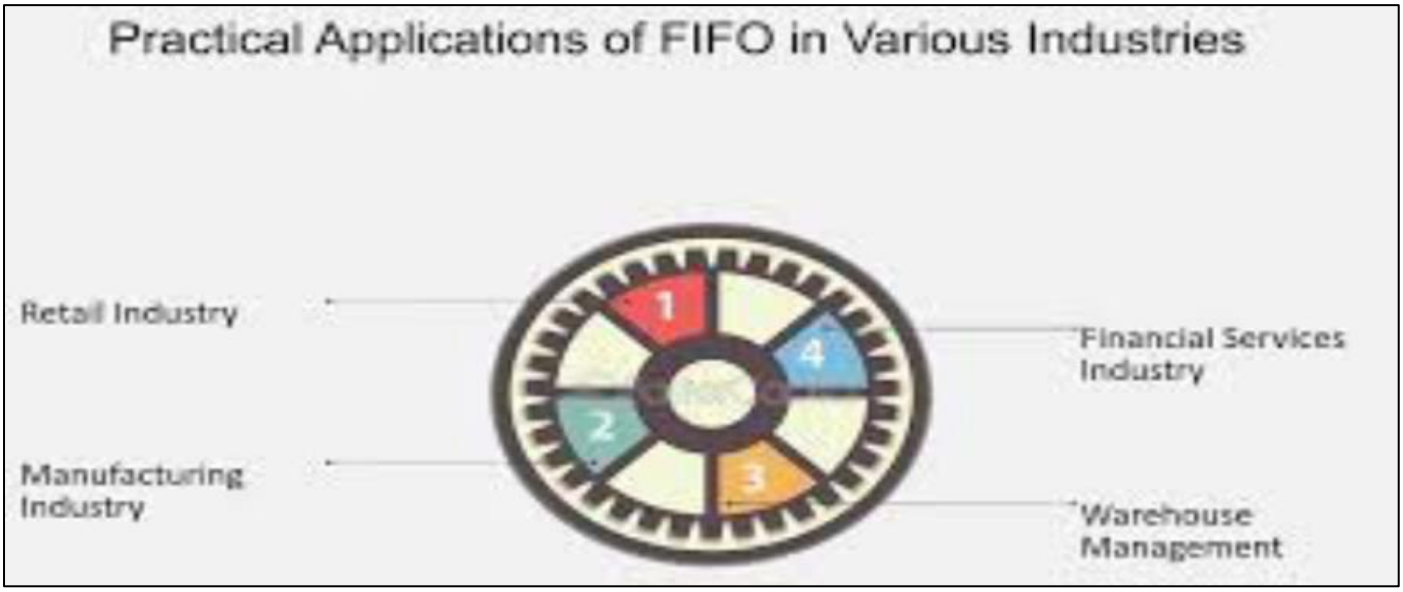

Fig 10 Various Applications of FIFO

ISSN No:-2456-2165 https://doi.org/10.5281/zenodo.14651164

➢ *Experimental Results*

The simulation of FIFO is first done to empirically assess the impact of FIFO implementation in manufacturing, a series of experiments were conducted in a simulated production environment. The experiments aimed to measure changes in production efficiency, work-in-progress (WIP) inventories, and overall operational performance following the adoption of FIFO principles. [8]

The following is the simulation waveform of FIFO given in the figure 6 Utilising the Cadence Genus synthesis tool, a gate-level netlist was derived from a functionally validated RTL de-sign, incorporating a 45 nm technology library and design constraints. This process yielded various reports, including a Synopsys Design Constraint (.sdc) file. Figure 4 illustrates the synthesised top-level schematic of the FIFO processor, featuring program counter, register, instruction, and ALU blocks.

IV. RESULT ANALYSIS

The results analysis primarily focuses on power and timing throughout the design flow as referred in Table I Power analysis includes various power reports, while timing analysis encompasses arrival time and slack. [4]

V. CONCLUSION

The findings of this research underscore the significant impact of First In, First Out (FIFO) implementation in manu-facturing environments.

$$F\,F\,GI(t) = F\,F\,GI(t-1) + P\,rod(t) - SoldF\,(t)Inv(t) \quad (1)$$

$$P\,F\,GI(t) = P\,F\,GI(t-1) + HeldInv(t) - SoldP.Inv(t) \quad (2)$$

$$P\,F\,GI(t) = P\,F\,GI(t-1) + HeldInv(t) - SoldP.Inv(t) \quad (3)$$

As we can see in equation (1),through a comprehensive ex-amination of theoretical frameworks, empirical evidence, and experimental results,we get the equation(2), equation(3), this study has demonstrated FIFO principles in streamlining pro-duction processes and minimising work-in-progress (WIP) inventories. [14] The empirical experiments conducted in simulated production environments have provided compelling evidence of the tangible benefits of FIFO implementation. Im-proved production efficiency, reduced cycle times, and lower WIP inventory levels are among the key outcomes observed following the adoption of FIFO practices. These findings not only reaffirm the theoretical advantages of FIFO but also offer practical insights for manufacturers seeking to enhance their inventory management practices and optimise production performance. [10]

ACKNOWLEDGEMENT

The author would like to thank Mohammed Abdul Raheem, Professor Electronics and Communication Department, for their time to time and proper guidance, continuous support and engagement in this research.

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