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An Exhaustive Review on Optimization of Carry-Look-Ahead Adder Using Hybrid Logic

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Abstract: A revolutionary method for designing contemporary digital circuits is the use of hybrid logic in the creation of carry-look ahead adders (CLAs), which combine CMOS and memristor technology. By combining the scalability and dependability of CMOS technology with the special qualities of memristors—such as their small size, low power consumption, and non-volatile nature—this review paper investigates developments in CLA architectures. The compiled studies demonstrate how hybrid memristor-CMOS designs can be used to get around drawbacks in conventional CLA implementations, such as decreased delay, power consumption, and circuit size. New approaches that show notable gains in processing efficiency and integration density include Memristor Ratioed Logic (MRL) and other creative hybrid approaches. These results highlight the potential of hybrid logic in creating carry-lookahead adders for next-generation computing systems that are both high-performing and energy-efficient.

Keywords: *CMOS, Memristor, Adder, MRL, CLA*

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I. INTRODUCTION

Optimizing arithmetic processes in digital circuits is a crucial endeavor in advancing modern computing systems. Among the various arithmetic units, the Carry-Lookahead Adder (CLA) is recognized for its ability to speed up the carry operation during binary addition. Traditional CLA designs, which rely on CMOS technology, have been widely adopted due to their scalability and well-established manufacturing processes. However, as the demand for higher-performance computing systems continues to rise, traditional CLAs face significant challenges. These challenges include maintaining high speed while minimizing area and power consumption, especially as circuits scale down to smaller technologies. The increasing complexity of digital systems necessitates more efficient approaches to overcome the limitations posed by conventional CMOS-based CLAs.

A promising solution to these challenges lies in the integration of memristor-based components with CMOS technology. Memristors, often referred to as the "fourth fundamental circuit element," are non-volatile devices that can store information without requiring continuous power. This ability to retain data without power makes them particularly attractive for use in digital circuits, as they can reduce power consumption and increase storage density. Unlike traditional memory elements, memristors have a unique characteristic that allows them to store data through the manipulation of their resistance. Their non-volatile nature, coupled with low power consumption and small physical size, makes them highly beneficial for improving the efficiency and performance of digital circuits. In this context, the combination of CMOS and memristors, known as hybrid memristor-CMOS logic, offers a novel approach that overcomes many of the limitations of traditional CMOS circuits.

The integration of memristors with CMOS technology allows for the creation of hybrid circuits that benefit from both the scalability and reliability of CMOS logic and the unique properties of memristors. One of the most significant benefits of using memristors in conjunction with CMOS is their ability to store data without the need for constant power, which is essential for minimizing power consumption in modern digital systems. By leveraging this property, hybrid circuits can be

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designed to achieve higher performance while simultaneously reducing power consumption, making them ideal for high-performance computing applications. Researchers have demonstrated that the combination of memristors and CMOS technology can lead to substantial improvements in the size, power efficiency, and speed of digital circuits, particularly in the design of CLAs [1].

The use of memristor-CMOS hybrid designs in CLAs has gained significant attention due to their ability to address the key limitations of traditional designs. Hybrid approaches, such as Memristor Ratioed Logic (MRL), have been explored as a means of reducing the circuit size while enhancing processing efficiency. MRL circuits, which leverage the unique properties of memristors, allow for more compact designs compared to traditional CMOS-based circuits. In addition to size reduction, MRL circuits also offer improvements in power consumption. By utilizing memristors to perform logic operations, the hybrid designs can significantly reduce the energy consumption of the circuits, making them more suitable for energy-efficient applications. These advancements are critical for the design of next-generation digital systems, where power efficiency, speed, and integration density are essential considerations [2].

Recent studies have shown that the use of memristor-CMOS hybrid designs in CLA circuits can significantly improve their overall performance. For example, hybrid memristor-CMOS CLAs have demonstrated reduced power consumption and faster processing times compared to traditional CMOS-based CLAs. This is particularly important for applications in high-performance computing, where speed and efficiency are paramount. As digital circuits continue to shrink in size, the need for more efficient designs becomes increasingly important. The combination of CMOS and memristors allows for the development of smaller, faster, and more energy-efficient circuits, addressing the challenges of modern digital systems. Researchers have highlighted the potential of memristor-based designs to improve the performance of CLAs by reducing the propagation delay associated with carry generation and propagation, a key bottleneck in traditional CLA designs [3].

One of the most significant advancements in the design of CLA circuits using memristor-CMOS hybrid technology is the development of memristor-based full adders. These full adders, which form the building blocks of CLAs, utilize memristors to perform addition operations more efficiently than traditional CMOS-based designs. Memristor-based full adders have been shown to consume less power and occupy less area than their CMOS counterparts, making them highly suitable for low-power and high-speed applications. Furthermore, the use of memristor-based devices allows for the creation of more compact and scalable full adders, which are essential for the design of large-scale digital systems. This represents a significant step forward in the development of energy-efficient digital systems, as reducing the size and power consumption of basic logic elements has a direct impact on the overall performance of the circuit [4].

The integration of memristors with CMOS technology holds significant promise for the design of next-generation digital systems. Hybrid memristor-CMOS CLA circuits offer a powerful solution to the challenges of high-performance computing, addressing the need for smaller, faster, and more energy-efficient circuits. By taking advantage of the unique properties of memristors, such as their non-volatility and low power consumption, these hybrid circuits can be used to develop more efficient and compact digital systems. As research in this area continues to progress, it is expected that memristor-CMOS hybrid designs will play a crucial role in the development of next-generation computing systems that are faster, more efficient, and more scalable. These advances in hybrid logic design will be instrumental in addressing the ever-increasing demands for high-performance computing, where speed, integration density, and energy efficiency are critical factors [5].

In summary, the combination of CMOS and memristor technology presents a revolutionary approach to digital circuit design, particularly in the design of carry-lookahead adders. By integrating the strengths of both technologies, researchers have been able to overcome many of the limitations of traditional CMOS-based circuits, paving the way for the development of smaller, faster, and more energy-efficient digital systems. As this field continues to evolve, the hybrid memristor-CMOS approach is expected to have a profound impact on the design of digital circuits, providing the necessary advancements to meet the growing demands of modern computing applications.

II. LITERATURE REVIEW

Recent years have witnessed tremendous progress in the field of digital logic design, with special focus on optimising adders—essential parts of arithmetic operations. The research articles reviewed here examine different methods for creating carry-lookahead adders (CLAs) with hybrid, CMOS, and memristor technologies. Every study offers a different perspective on the possible advantages and difficulties of these cutting-edge methods.

An advanced memristor model is suggested by P. Shivani Reddy et al [1]. to design a carry-lookahead adder (CLA). Because of their high processing speed and energy economy, memristors—which store and process information based on resistance—are being included into digital circuits more and more. The study suggests a "improvised" memristor model that improves the CLA's performance by lowering power consumption and propagation latency, two crucial elements of digital arithmetic circuits. The authors hope to get around some of the drawbacks of conventional CMOS-based adders by utilising the special qualities of memristors.

Hybrid CMOS-Memristor Approach for Carry-Lookahead Adder (CLA)Gongzhi Liu et al [2]. In order to create a more effective carry-lookahead adder (CLA), the authors of this paper investigate the combination of CMOS and memristor-based logic circuits. The hybrid CMOS-memristor approach combines the advantages of both technologies, where memristors help to reduce power consumption while CMOS provides high-speed switching. In contrast to traditional CMOS-based adders, this design minimizes energy consumption while achieving faster computation times, addressing the trade-offs between performance and energy efficiency.

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Comparative Study of Logic Design Methods for RCA and CLA by Kuldeep Singh Shekhawat et al [3] In the context of ripple carry adders (RCA) and carry lookahead adders (CLA), this study compares several logic design methods, including CMOS, Gate Diffusion Input (GDI), Transmission Gate (TG), and Enhanced Charge Recycling Logic (ECRL). The authors examine the trade-offs of each technology, with a particular focus on power consumption, speed, and area. The study highlights how TG and ECRL are advantageous for high-speed applications, while ECRL and GDI technologies may outperform conventional CMOS in some areas, especially in low-power designs.

Hybrid Memristor-CMOS Implementation of Logic Gates Design Using LTSpice by Wan Mohd Hashimi et al [4]. This research utilizes LTSpice simulation tools to study the hybridization of memristor and CMOS technologies, with a focus on logic gate design. The authors emphasize the design of basic logic gates, which serve as building blocks for more complex circuits, such as adders. The hybrid architecture is ideal for low-power and small devices, as it significantly reduces both area and power consumption. Additionally, the use of LTSpice simulation enables a thorough examination of circuit behavior, providing valuable insights into the practical application of memristor-based designs in real-world settings.

MRL – Memristor Ratioed Logic by Shahar Kvatinsky et al [5] By using memristors to lessen the requirement for intricate transistor-based logic architectures, the Memristor Ratioed Logic (MRL) paradigm for digital circuit design is presented in this work. In order to create effective circuits without heavily depending on conventional voltage-based logic, MRL focusses on controlling the current flowing through logic gates using memristor ratios. Because it investigates how memristors might be used to develop whole new logic families that are possibly quicker and more energy-efficient than traditional CMOS logic, this work is noteworthy.

Multi-input Memristor Rationed Logic Full Adder Circuit for Efficient Processing Time by Suparlerk Yamtim et al [6]. This study explores the use of multi-input memristor-ratioed logic (MRL) to enhance processing time efficiency in full adder designs. The authors minimize area and power consumption while achieving faster computation times in the adder circuit by utilizing a multi-input technique. Furthermore, the work highlights how multi-input logic can optimize the efficiency of full adders, which are critical components of processor arithmetic units. The integration of memristor technology in this context holds potential for improving the speed and efficiency of arithmetic circuits.

Design and Analysis of Carry Lookahead Adder Using CMOS Technique by Amita, Mrs. Nitin Sachdeva [7]. This work addresses carry propagation delays, a critical limitation in high-performance computing systems, in order to optimize addition speed. The authors preserve power and space constraints while enhancing operating efficiency through CMOS design techniques. The study provides insights into the practical application of carry lookahead adders (CLAs), demonstrating how CMOS designs can balance silicon area, speed, and power consumption, making them suitable for a wide range of digital applications.

Optimized Implementation of Memristor-Based Full Adder by Material Implication Logic by Mehri Teimoory et al [8]. This study highlights the advantages of memristor technology, including its scalability, non-volatility, and low power consumption. By employing material implication logic, the authors propose a compact solution that consumes less area and energy compared to conventional CMOS-based adders. The research positions memristors as a promising alternative for next-generation arithmetic circuits and underscores their potential in advancing computing paradigms.

Memristor: The Missing Circuit Element by Leon O. Chua [9]**.** In his seminal work, Leon Chua presents the idea of the memristor as the fourth essential passive circuit component, after resistors, capacitors, and inductors. Based on past charge flow, this study establishes the theoretical foundation for the memristor, which is distinguished by its capacity to maintain resistance states. Chua bridges the gap between memory and logic functionalities with his work, offering a revolutionary viewpoint on circuit design. As a result of this discovery, a great deal of research has been done on neuromorphic computing, non-volatile memory architectures, and memristor-based computing systems.

CMOS-Based Memristor Emulator Circuits for Low-Power Edge-Computing Applications by Prosenjit Kumar Ghosh et al [10]. The authors create compact and low-power solutions that are appropriate for edge devices with limited resources by simulating memristive behaviour within CMOS circuits. In order to provide memristor-like functionalities without the need for hardware memristors, this work demonstrates the practical difficulties and solutions. The suggested circuits open the path for improvements in edge computing technologies by showcasing their usefulness in real-time processing workloads and neuromorphic computing.

Area & Power Optimized Hybrid CMOS-Memristor Logic Circuit Based Carry Look-Ahead Adder by Manimegalai Munisamy, Janani Munisamy v [11]. In order to create a carry look-ahead adder, Munisamy and Munisamy investigate a hybrid design method that blends CMOS and memristor technology. The hybrid design makes use of both technologies' advantages: memristors' small size and energy efficiency and CMOS's fast speed of operation. When compared to traditional implementations, their concept delivers notable reductions in both area and power usage. This work provides a convincing answer for applications needing high-performance and energy-efficient arithmetic units by proving the viability and advantages of hybrid circuits.

III. PROPOSED WORK

The research has focused on optimising the Carry-Look-Ahead (CLA) Adder because of its critical function in high-speed arithmetic operations, especially in contemporary computer systems. Significant obstacles frequently confront traditional methods to CLA design, such as excessive power consumption, increased propagation latency, and scalability constraints, particularly as bit-width increases. These drawbacks reduce CLA circuits' effectiveness in sophisticated applications that need for quick and precise computations. In order to tackle these problems, this research suggests a thorough approach for improving CLA performance.

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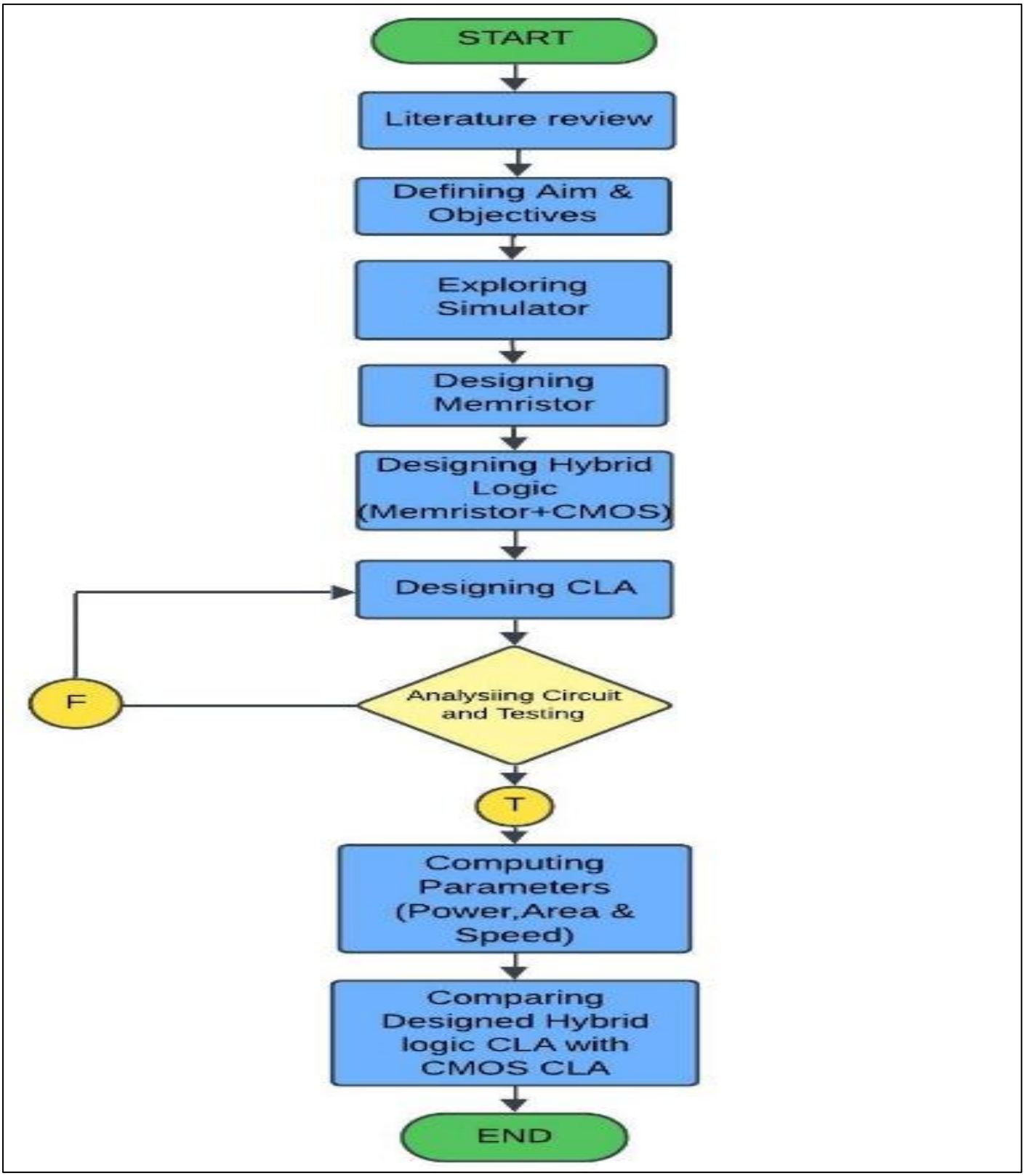

Fig 1 Flowchart Showing Step by Step Processchalo

The proposed workflow for designing and analyzing a novel hybrid logic-based Carry Look-Ahead (CLA) circuit integrates memristor technology with CMOS logic. The process is as follows:

- Literature Review: Conduct an extensive review of existing research to understand the state-of-the-art in memristor technology, CMOS logic, and hybrid circuits. This helps identify gaps and set the foundation for innovative contributions.
- Defining Aim and Objectives: Clearly define the goals of the study, emphasizing the improvement of performance metrics such as power consumption, area efficiency, and speed. The objectives guide the overall research and experimentation process.

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- Exploring Simulator: Select and familiarize with simulation tools capable of modeling both memristor-based and CMOS circuits. The simulator must support hybrid logic designs and provide accurate performance parameter outputs.
- Designing Memristor: Develop the memristor model to be used in the hybrid logic. This step involves configuring the electrical and behavioral properties of the memristor for integration into the hybrid circuit.
- Designing Hybrid Logic (Memristor + CMOS): Combine the memristor model with CMOS logic to create a hybrid logic circuit. This innovative design aims to leverage the strengths of both technologies, such as reduced power consumption from memristors and reliable operation from CMOS.
- Designing CLA: Implement the hybrid logic in the Carry Look-Ahead (CLA) circuit. The CLA is chosen for its efficiency in high-speed arithmetic operations.
- Analyzing Circuit and Testing: Perform detailed circuit analysis and rigorous testing to validate the functionality of the hybrid CLA design. Iterative testing ensures the design meets the predefined objectives. If the results are unsatisfactory, the circuit is refined and reanalyzed.
- Computing Parameters: Evaluate critical performance parameters, including power consumption, area utilization, and operational speed. These metrics quantify the advantages of the hybrid design.
- Comparing Designed Hybrid Logic CLA with CMOS CLA: Benchmark the performance of the proposed hybrid CLA against a conventional CMOS-only CLA design. The comparison highlights the improvements achieved through the hybrid approach.
- End: Summarize the findings and document the design, testing, and comparison results. This step concludes the proposed workflow and establishes the contribution of the study.

➢ *Problem Identification*

Compared to ripple-carry adders, Carry-Look-Ahead Adders (CLAs) are employed extensively in arithmetic operations because of their quick carry propagation, which cu ts down on calculation time. As the bit-width grows, though:

- Propagation delay: Rises as a result of carry propagation logic constraints.
- Power consumption: Increases significantly, particularly in applications involving huge amounts of data.
- Area Overhead: Scalability and energy efficiency are restricted by the huge number of transistors needed for traditional CMOS solutions.

These problems have been partially resolved by existing methods, such as employing different logic gates or lowering transistor counts, but they frequently involve trade-offs between area, power, and speed. Additionally, memristor-based logic has potential for processing that uses less energy, but it is not integrated into a workable CLA design framework.

➢ *Proposed Optimization Framework*

This work proposes a detailed, modular design for optimizing the CLA Adder by incorporating hybrid logic. The following blocks are targeted for improvement:

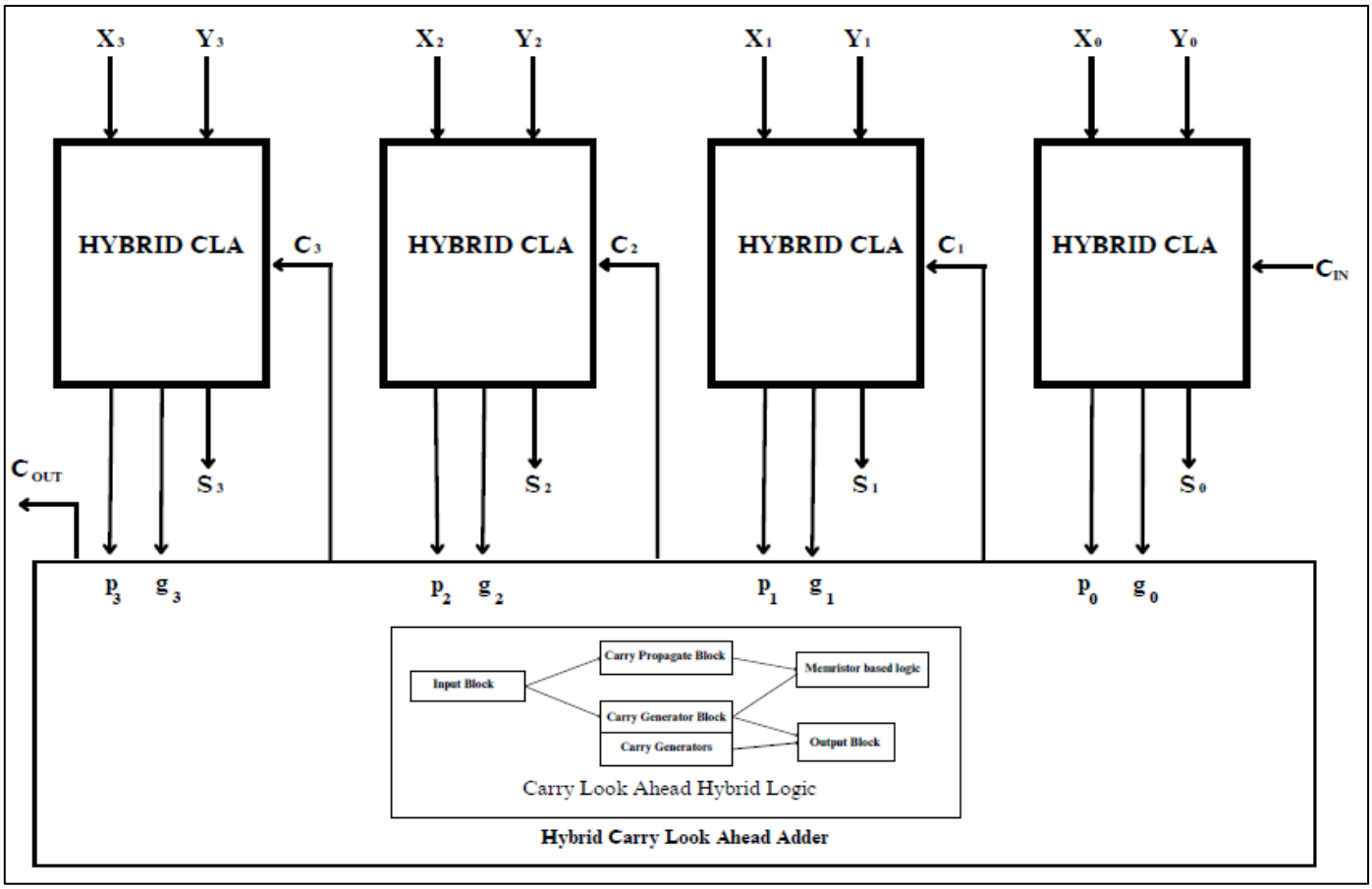

Fig 2 Block Diagram - Carry Lookahead Adder (CLA)

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➢ *Input Block*

- The input block is designed to process the binary inputs (X and Y) using hybrid logic gates.
- The hybrid gates aim to reduce power leakage while ensuring precise signal transmission to subsequent stages.

➢ *Carry Propagation Block*

- In this block, hybrid logic is employed to optimize the generation of carry propagate (P) and carry generate (G) signals.
- The logic reduces the critical path delay, ensuring faster signal processing.

➢ *Carry Generator Block*

- A key innovation in this framework is the integration of memristor-based logic in the carry generator block.
- Memristors offer advantages such as lower power consumption, reduced area, and non-volatile memory, enabling efficient carry generation.

➢ *Output Block*

- The summation process is enhanced using hybrid logic gates that ensure robust computation of the sum bits with minimal delay.
- This block also integrates mechanisms to maintain consistency and accuracy in the final output under high-speed operations.

IV. METHODOLOGY

➢ *The proposed work follows a structured methodology:*

- Hybrid Logic Design**:** Develop optimized hybrid logic gates tailored for each block of the CLA.
- Memristor Implementation**:** Design and test memristor-based logic components for the carry generator block using simulation tools.
- Simulation and Testing**:** Evaluate the proposed design using standard simulation platforms to measure key performance metrics such as:
- Power-Delay Product (PDP)**:** To quantify the trade-off between power and speed.
- Energy-Delay Product (EDP)**:** To evaluate overall energy efficiency.
- Area Efficiency**:** By analyzing the transistor and memristor counts in the design.
- Comparative Analysis**:** Compare the proposed design against existing CLA implementations to highlight improvements.

V. EXPECTED OUTCOMES

➢ The proposed hybrid logic-based CLA design is expected to achieve:

- Reduced Propagation Delay**:** By optimizing the carry propagation and summation logic.
- Improved Power Efficiency**:** Through the use of memristor-based logic in key blocks.
- Enhanced Area Efficiency**:** By reducing the number of transistors and leveraging the compact nature of memristors.
- Scalability**:** A modular architecture that supports higher bit-width operations while maintaining performance metrics.

VI. CONCLUSION

The proposed work highlights the promising advancements in carry-lookahead adder (CLA) design enabled by the integration of hybrid CMOS-memristor and memristor-based technologies. Traditional CMOS circuits face inherent limitations in speed, power consumption, and area efficiency, which hinder their performance in high-speed applications. Memristors offer an innovative solution to these challenges, providing the potential for more compact and energy-efficient designs. However, their widespread adoption is still limited due to issues such as resistance drift, nonlinear behavior, and the complexity of optimizing hybrid circuits. The hybrid CMOS-memristor approach presents a compelling strategy to overcome these obstacles and develop high-performance, low-power adders with improved area efficiency. Future research should focus on addressing these issues by refining simulation models, enhancing memristor-based design techniques, and optimizing the integration of CMOS and memristor components. Such efforts will be essential for unlocking the full potential of memristor-enhanced digital circuits, paving the way for their application in next-generation computing systems and beyond.

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