Volume 9, Issue 10, October – 2024 International Journal of Innovative Science and Research Technology
ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/IJISRT24OCT451

Comparative Study and Simulation of ADC Using MATLAB/SIMULINK

Youssef. N. Amhamad[1]; ALMUKHTAR AHMED[2]
[1]Faculty of Technical Sciences, Sebha – Libya
[2]Electrical &Electronics Department Faculty of Engineering Sabratha, Sabratha University, Sabratha- Libya

Abstract:- Digital systems play an important role in science and engineering field due to high noise immunity,high accuracy and required less space for data storage. And since all physical quantities are available in analog form so we need device which convert these quantities into digital one this device is called analog to digital converter (ADC).In this paper we present and simulate model for ADC using MATLAB/SIMULINK .

Keywords:- *Sampling, Quantization, Encoder, MATLAB/SIMMULATION.*

I. INTRODUCTION

The majority of physical variables that are encountered in daily life are analog in nature and can have any value within a continuous range, such as temperature, pressure, light intensity, audio signals, etc[1,5]. All internal operations of digital systems are, however, carried out by digital circuitry; any data that has to be entered into a digital system must first be transformed into a digital format, and outputs are always in digital format [2]. It is therefore necessary to transfer the data from one form to another in order to interface the analog and digital systems. Four steps must be taken in order to convert an analog signal to a digital format: sampling, holding, quantizing, and encoding as shown in Fig1. In this case, a sample and hold circuit (S/H) is used to sample and hold concurrently [6]. Using a circuit known as an analog to digital converter, the quantization and encoding procedures are carried out concurrently.

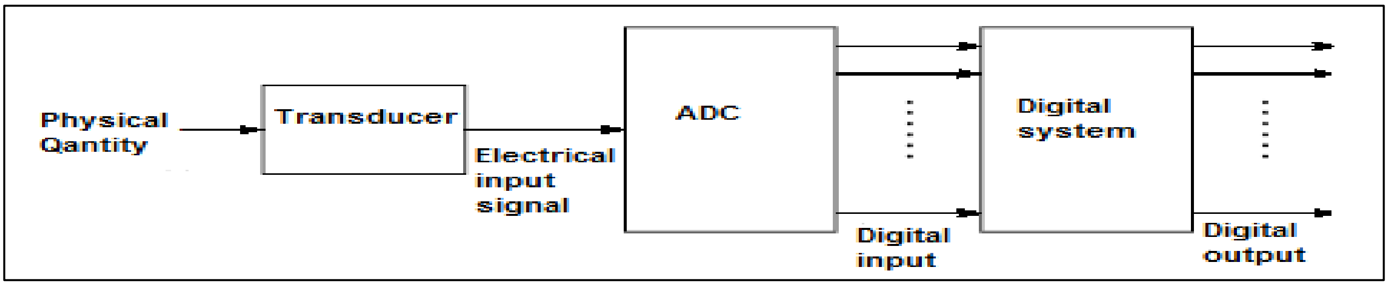

Fig 1: ADC Interface

A. Types of A to D Converters:

- *Digital Ramp.The Schematic Diagram is Shown in Fig2*

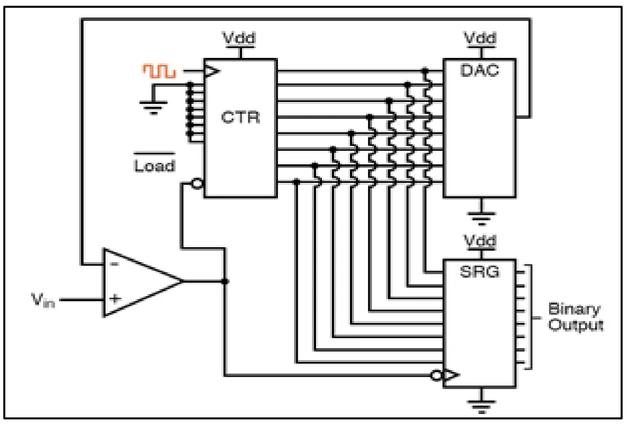

Fig 2: Digital Ramp ADC

- *Successive Approximation A To D Converter. The Scematic*

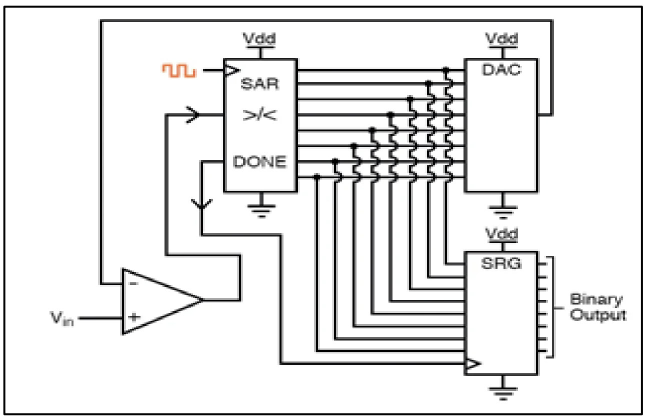

Fig 3: Successive Approximation A/D

ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/IJISRT24OCT451

- *Slope(Integrating Type) A to D Converter.The Schematic Diagram is Shown in Fig4*

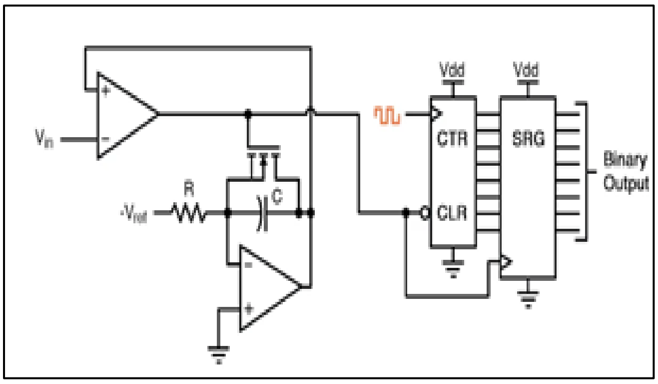

Fig 4: Slope Type ADC

- *Delta __ Sigma A to D Converter. The Schematic Diagram is Shown Un Fig5*

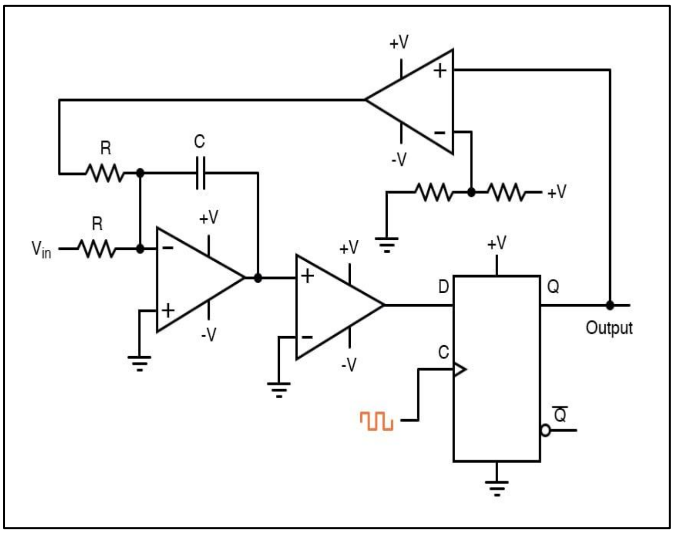

Fig 5: Delta __ Sigma A to D Converter

- *Flash Type.The Schematic Diag Is Shown In Fig6*

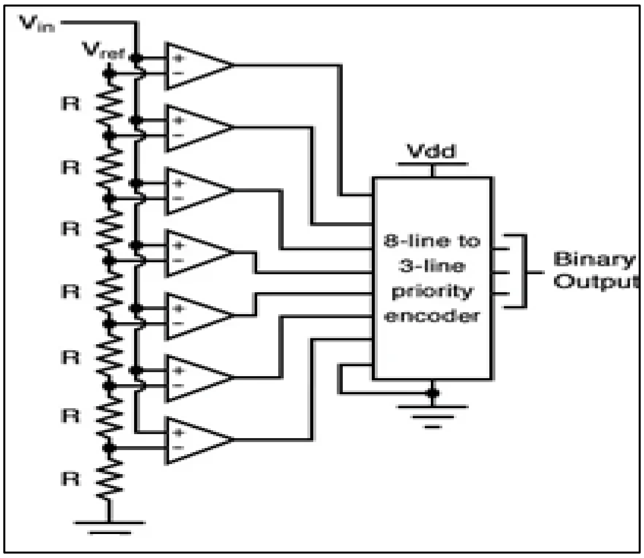

Fig 6: Flash Type ADC

- *Tracking Type*

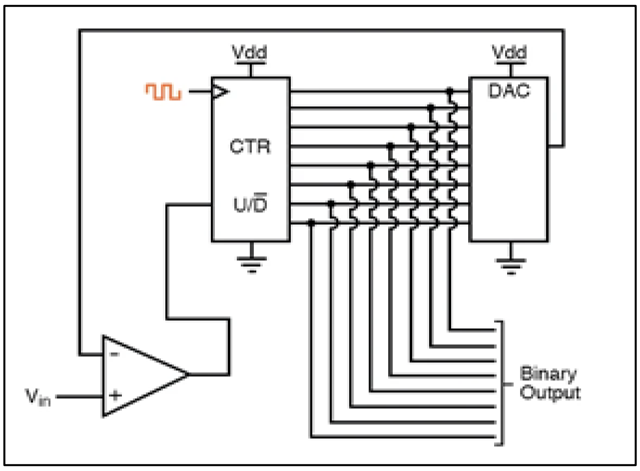

Fig 7: Tracking Type ADC

B. ADC Selection;

- The number of bits (higher number of bits better is the resolution)
- Accuracy.
- Speed of conversion.
- Range of the input signal.

C. ADC Characteristics:

- Resolution which is the maximum number of digital output codes.
- Conversion time which is the total time required to convert the analog input signal into corresponding digital output.
- Quantization error the digital output is not always the accurate representation of the analog input for instance any input voltage between 1/8 to 2/8 of full scale will be converted to a digital word of 001 this approximation process is called as quantization and the error due to the quantization process is called as quantization error as shown in fig8.

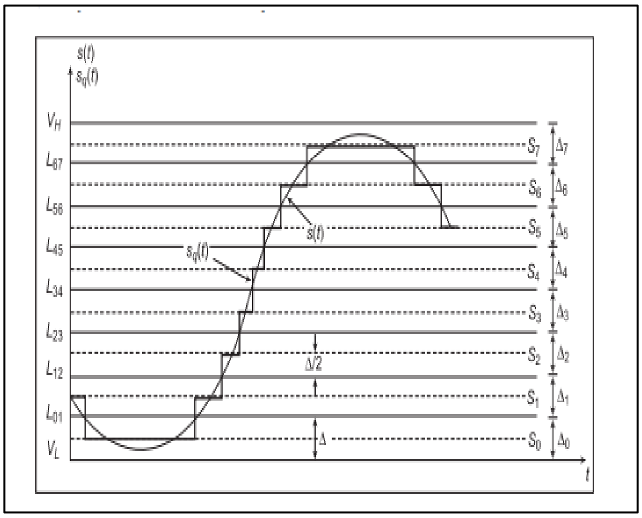

Fig 8: Quantization

* *Sample and Hold Circuit*

Maintaining a consistent analog input voltage during the conversion process is essential for efficient analog to digital conversion. The digital output code has an error if the analog input voltage varies by more than + or - LSB. We employ a sample and hold (S/H) circuit because it is vital to maintain the analog input voltage value throughout the conversion process in order to reduce the possibility of these errors. As seen in Figure 7, the sample and hold circuit samples the input signal value in response to the sampling command and holds it at the output until the next instruction is received [5]. It takes extremely little time to sample an analog input voltage. The response of the input and output of (S/H)) circuit is shown in Fig 9.

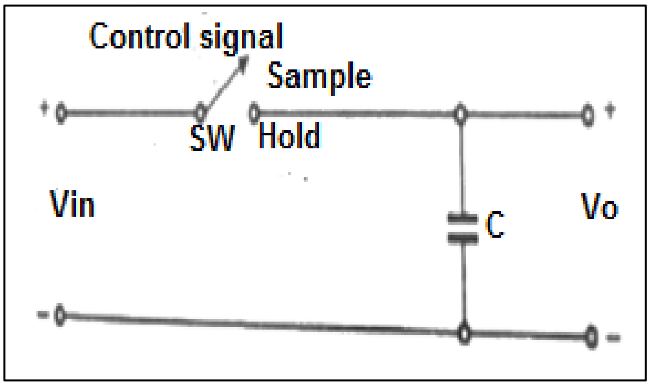

Fig 9: Sample and Hold Circuit

D. Summary of Different ADC Types Ranked From Best to Worst are Shown In Table 1:

Table 1 Summary of Different ADC Types

Rank	Speed	Resolution	Step recovery
1	Flash	Single Slpoe	Flash
2	Tracking	Dual slope	Successive approxi.
3	Successive approxi.	Counter	Single Slope
4	Single slope & Counter	Tracking	Dual slope &Counter
5	Dual slope	Successive approxi.	Tracking
6		Flash	

➢ *Developed Model*

* *The Model is Developed using MATLAB/SIMULINK is Shown in Fig 10:*

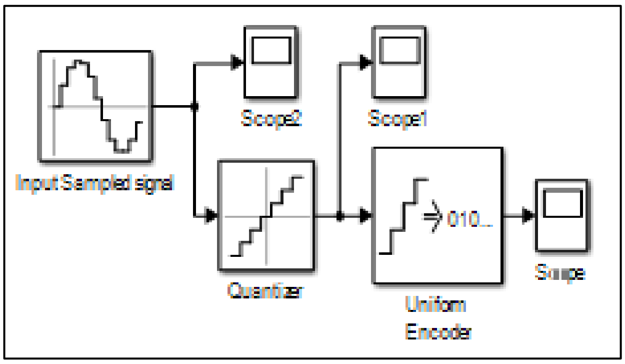

Fig 10: ADC Model

II. SIMULATION RESULTS

The model is simulated with sampling time 0.2s and Quantization levels 0.2,0.15,0.13 respectively and then with sampling time 0.3s and Quantization levels 0.2,0.15,0.13 respectively and the results are shown below:

➢ *Sampling time 0.2S, Quantization level (0.2,0.15,0.13) Encoder a1.*

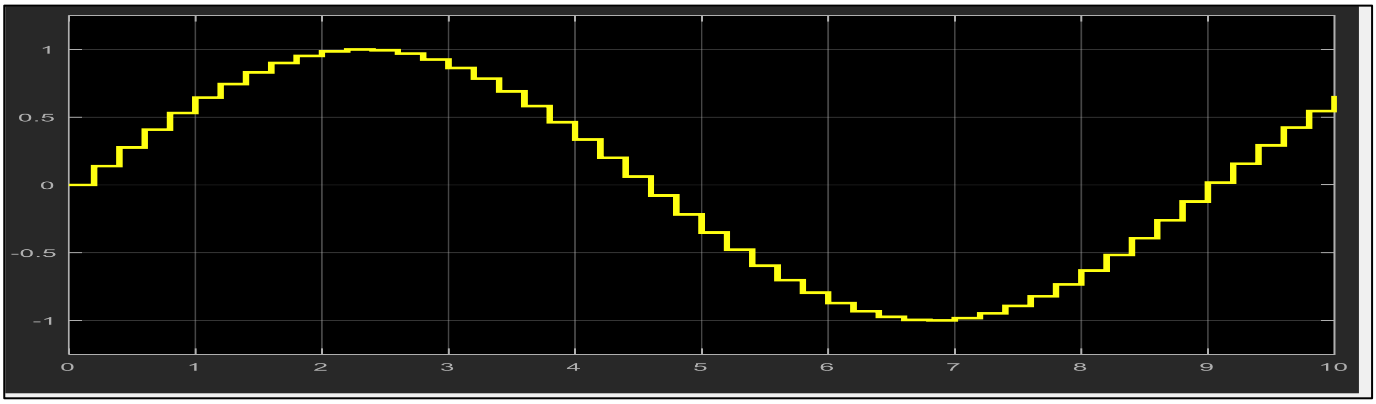

Fig 11: Input Sampled Signal(0.2s)

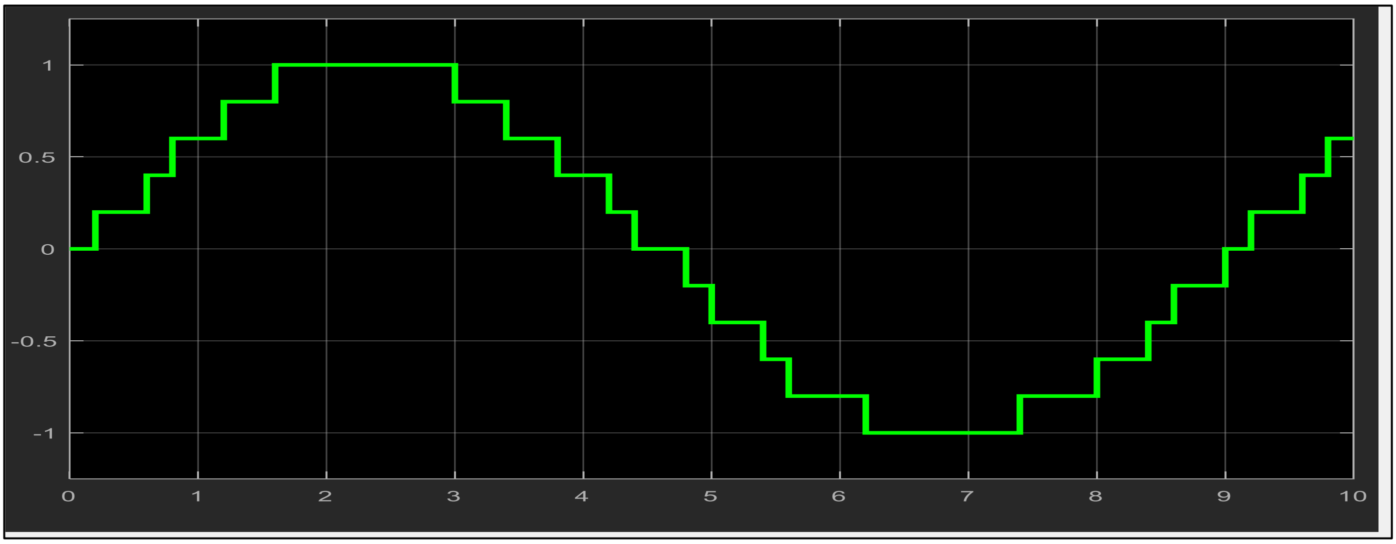

Fig 12: Quantizer Output (0.2)

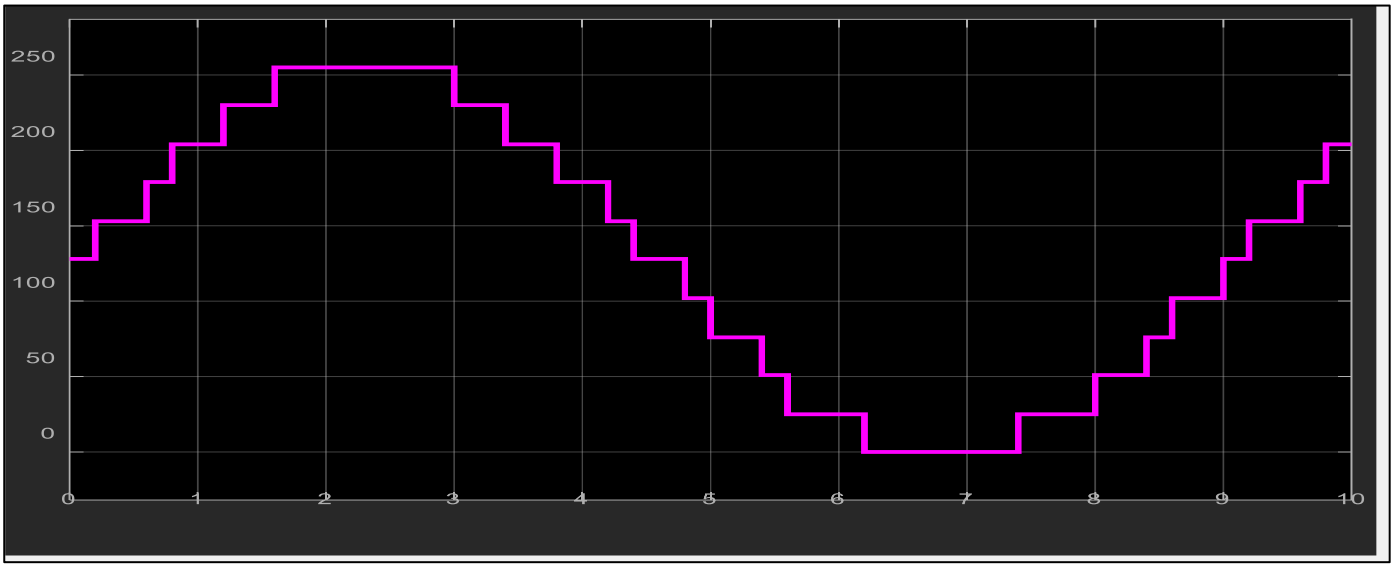

Fig 13: Encoder Output (Peak Value1)

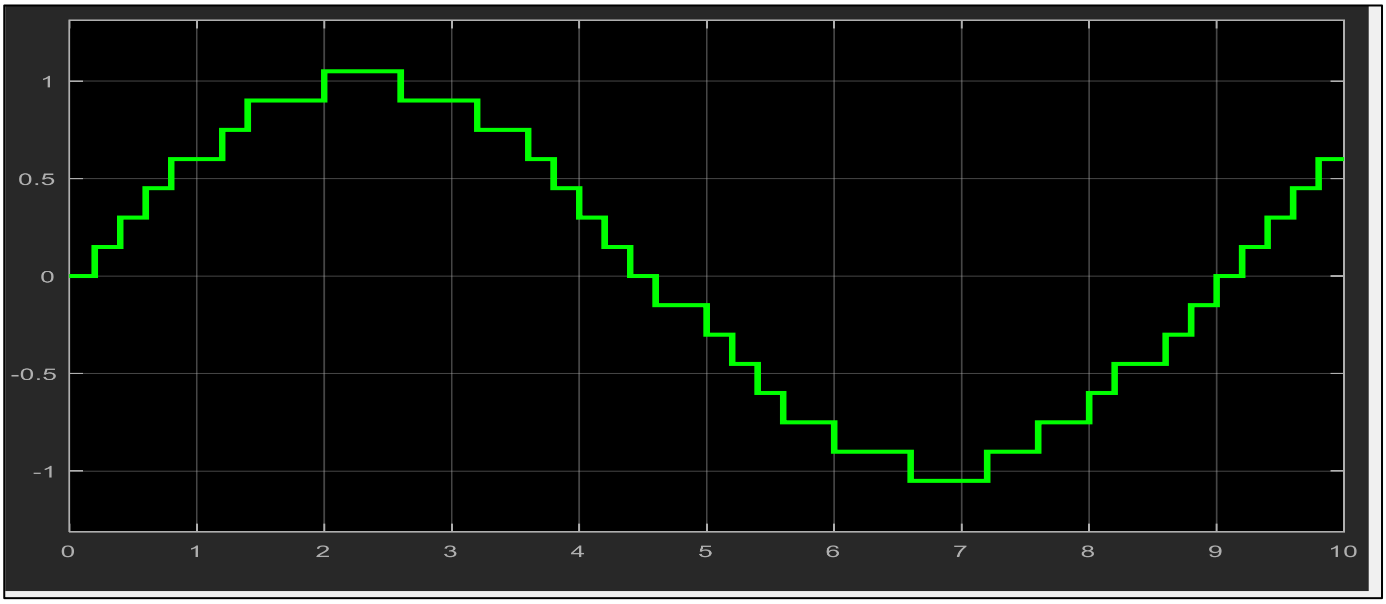

Fig 14: Quantizer Output (0.15)

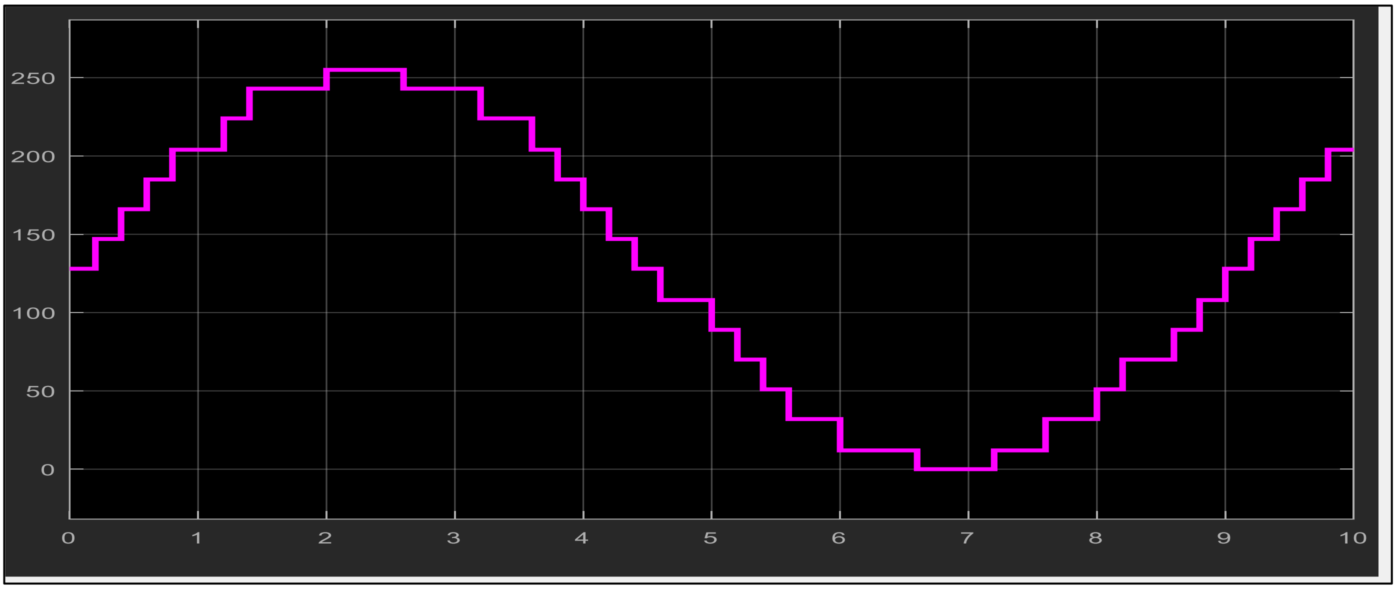

Fig 15: Encoder Output (1)(0.15 Quant.)

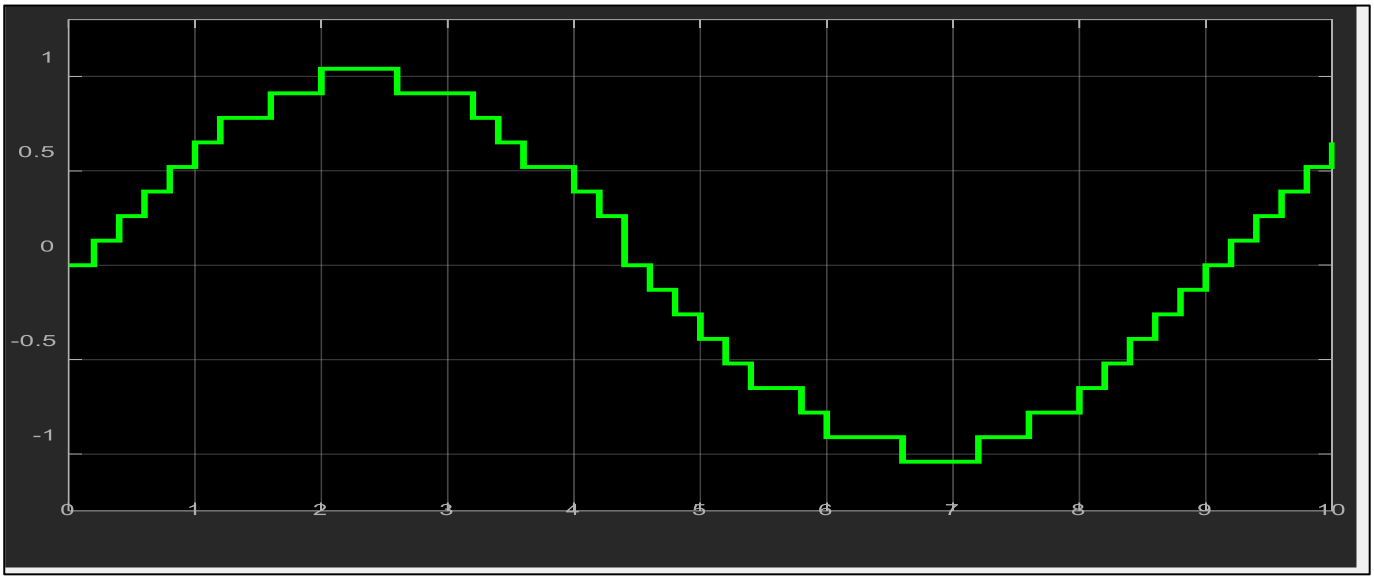

Fig 16: Quantizer Output (0.13)

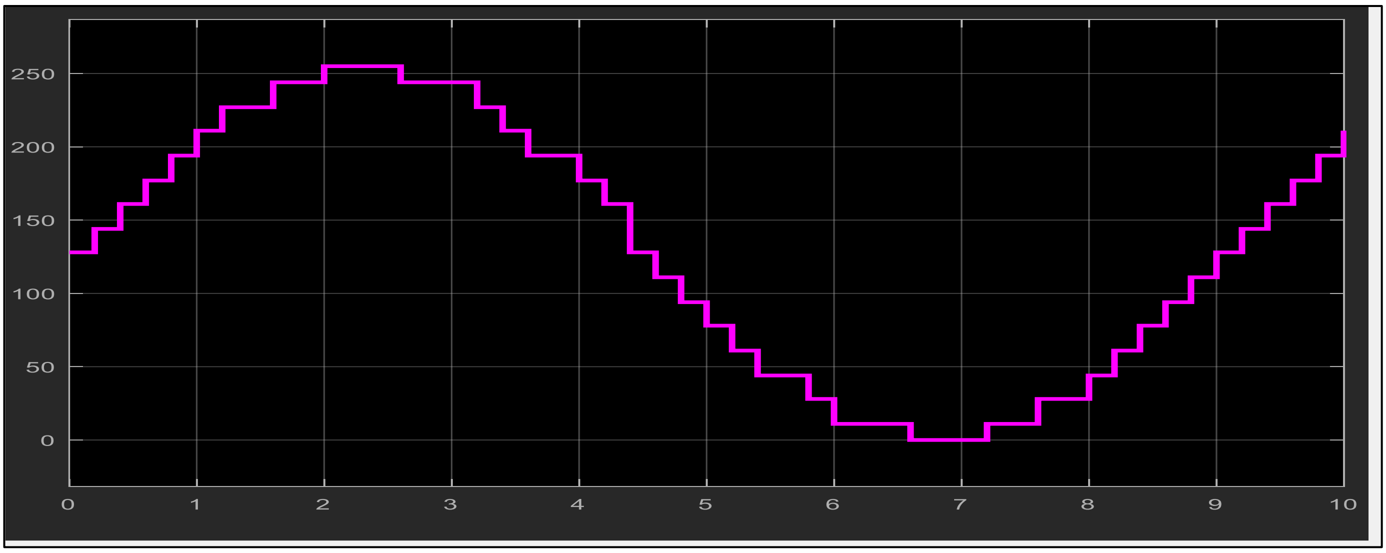

Fig 17: Encoder Output (1)(0.13 Qant.)

➢ *Sampling Time 0.3S , Quantization Level (0.2,0.15,0.13) Encoder Peak Value 1.*

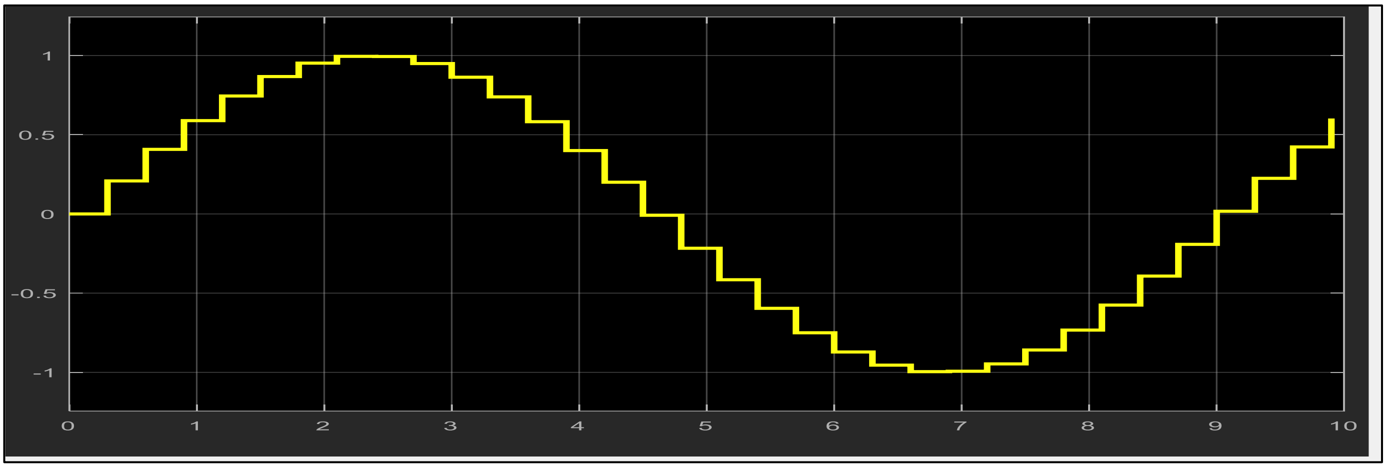

Fig 18: Input Samples Signal 0.3S

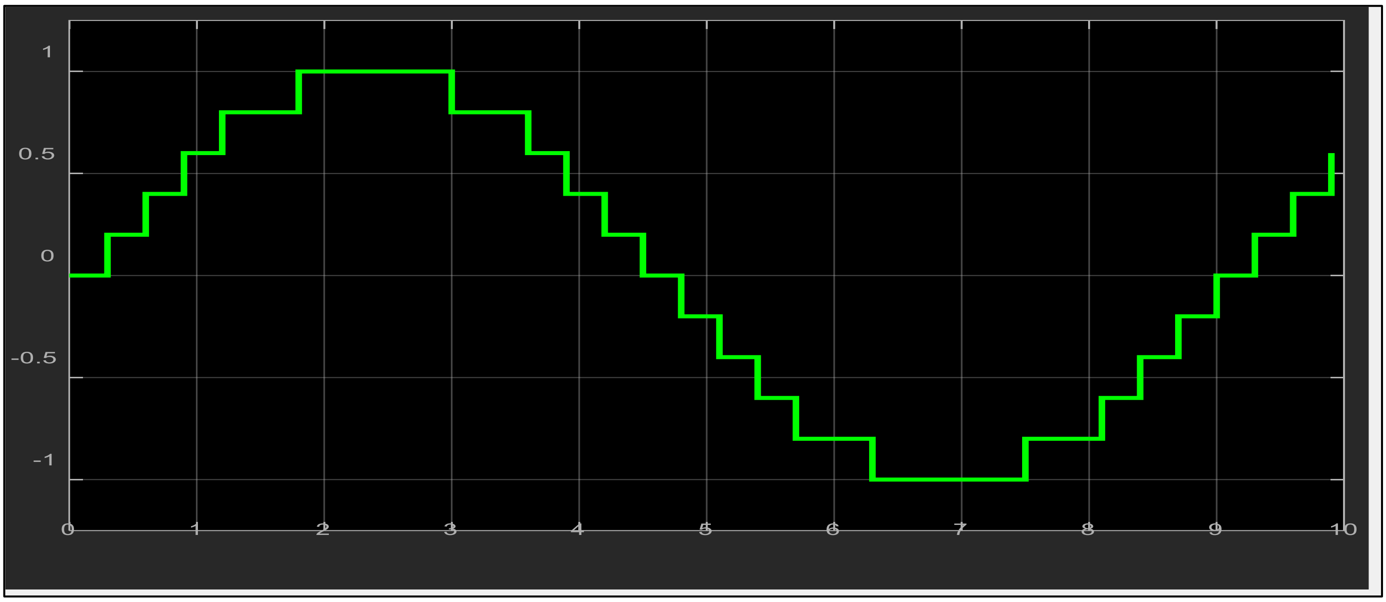

Fig 19: Quantizer Output (0.2)

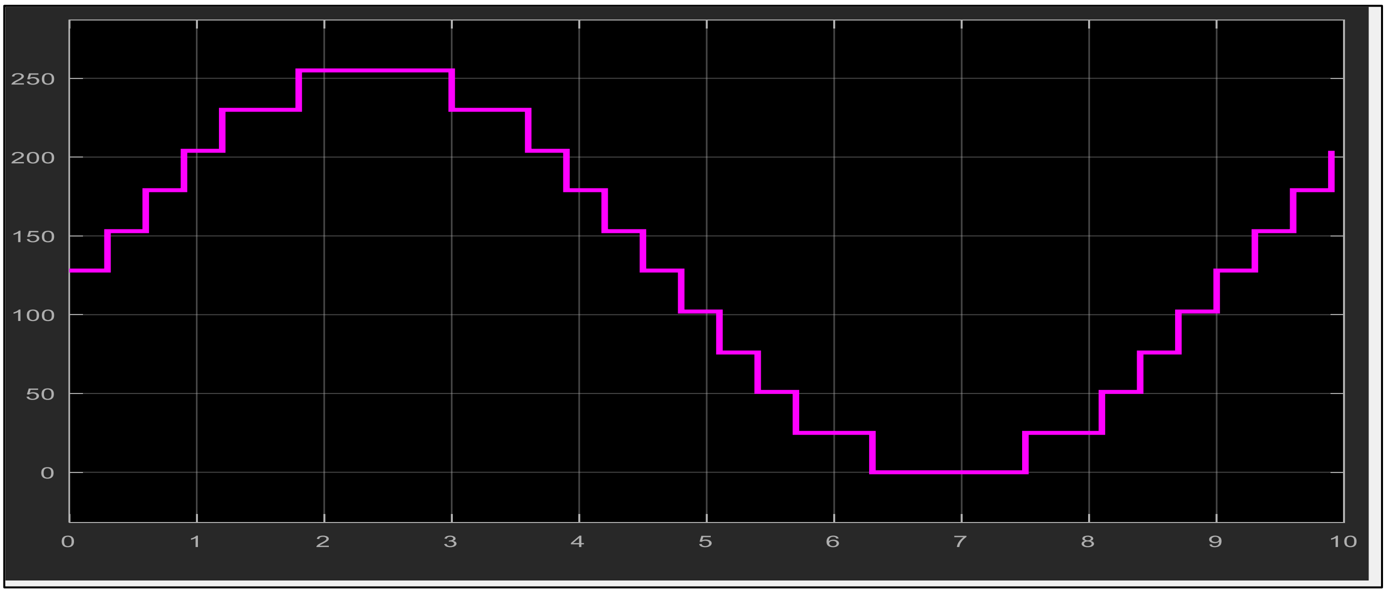

Fig 20: Encoder Output (1)(0.2 Qant.)

ISSN No:-2456-2165
https://doi.org/10.38124/ijisrt/IJISRT24OCT451

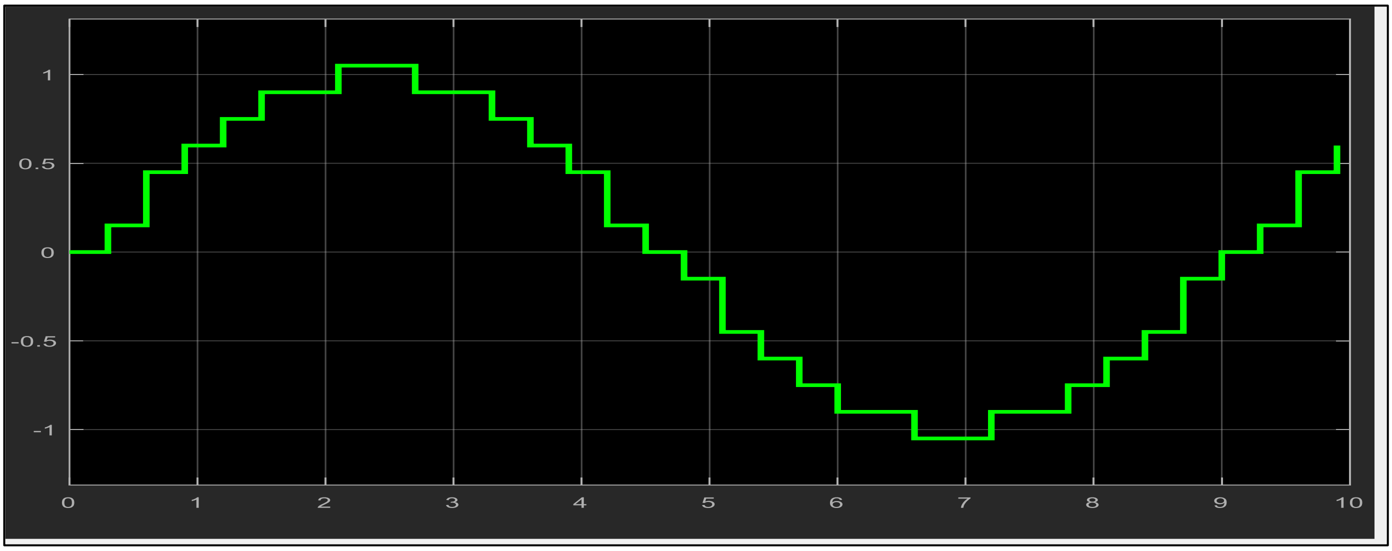

Fig 21: Quantizer Output (0.15)

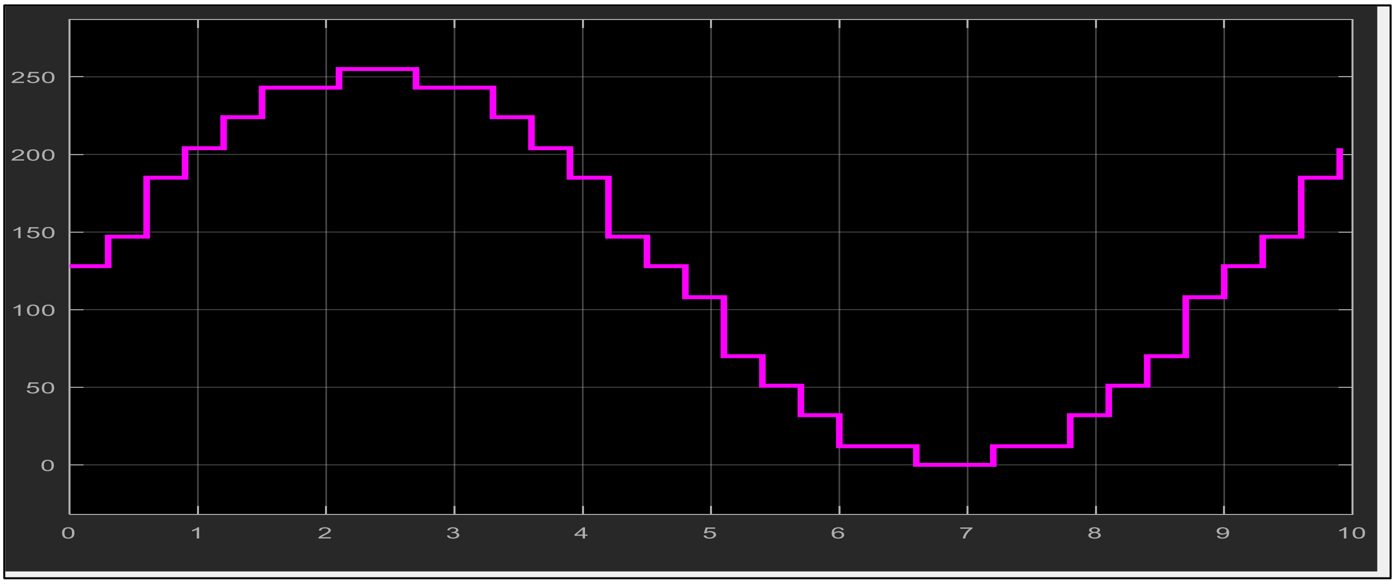

Fig 22: Encoder Output (1)(0.15)

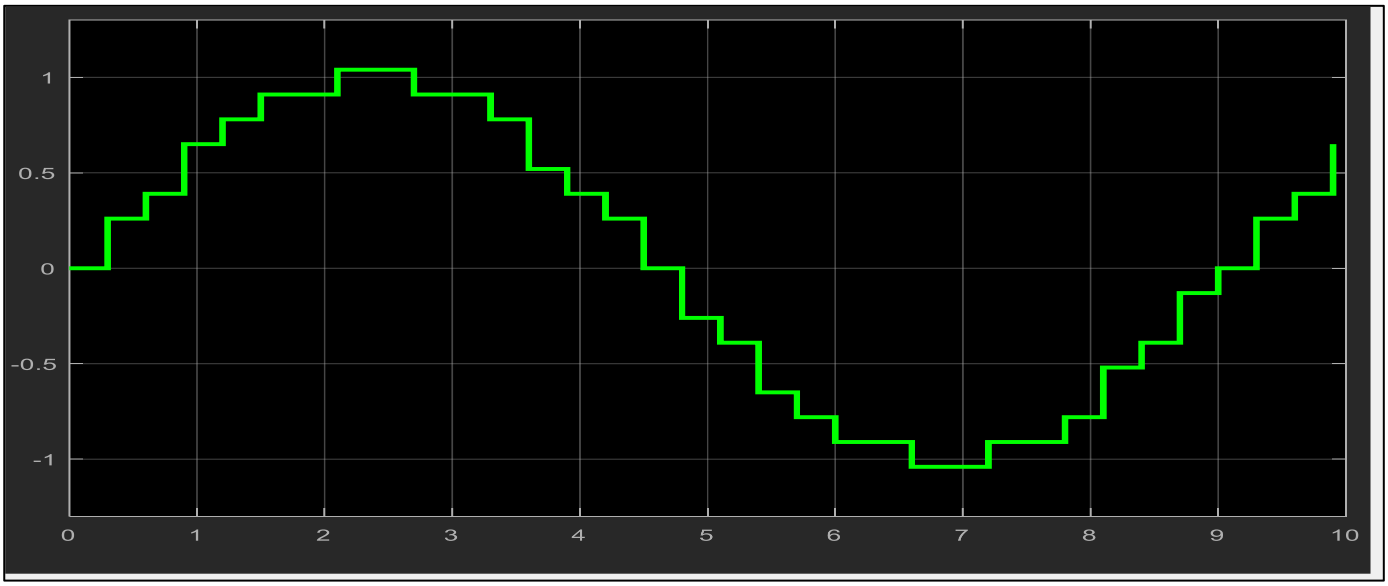

Fig 23: Quantization Output (0.13)

ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/IJISRT24OCT451

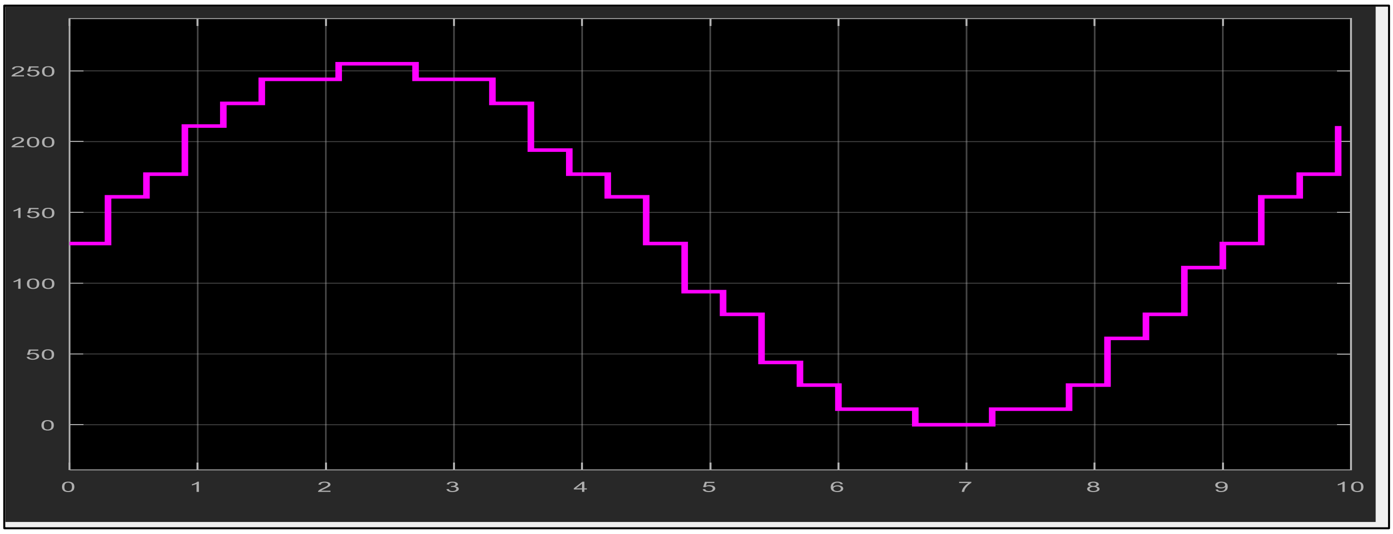

Fig 24: Encoder Output (1)(0.13)

➢ *Sampling Time 0.3s , Quantization Level (0.2,0.15,0.13) Encoder Peak Value 2.*

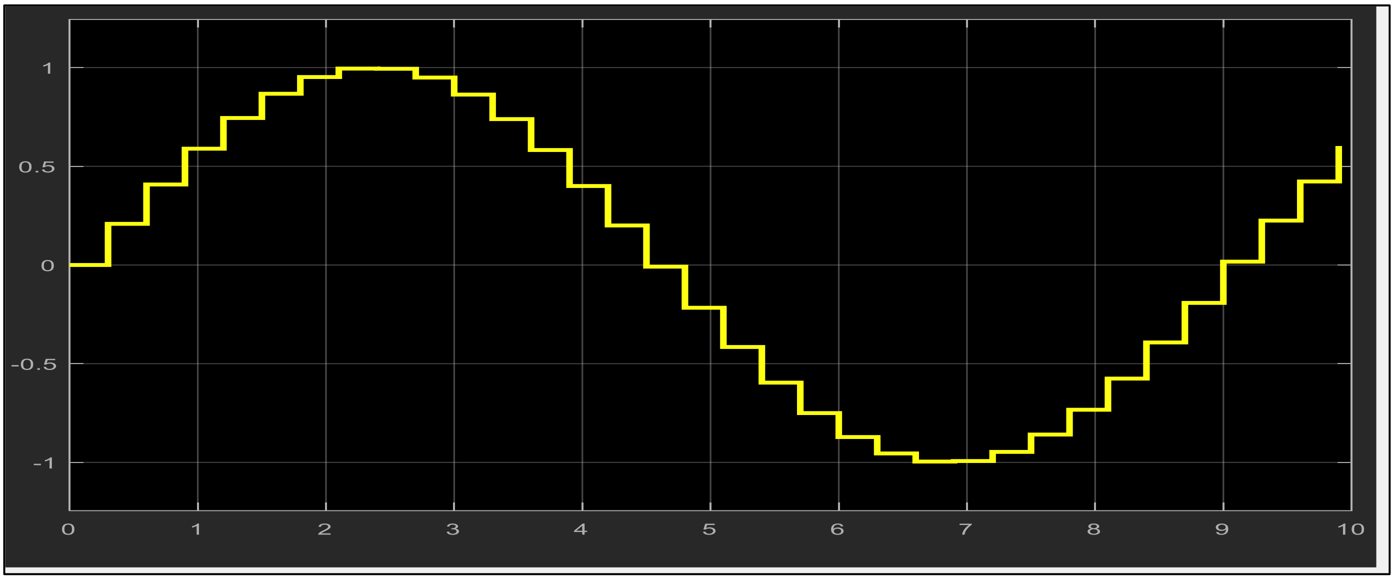

Fig 25: Sampled Signal 0.3 S

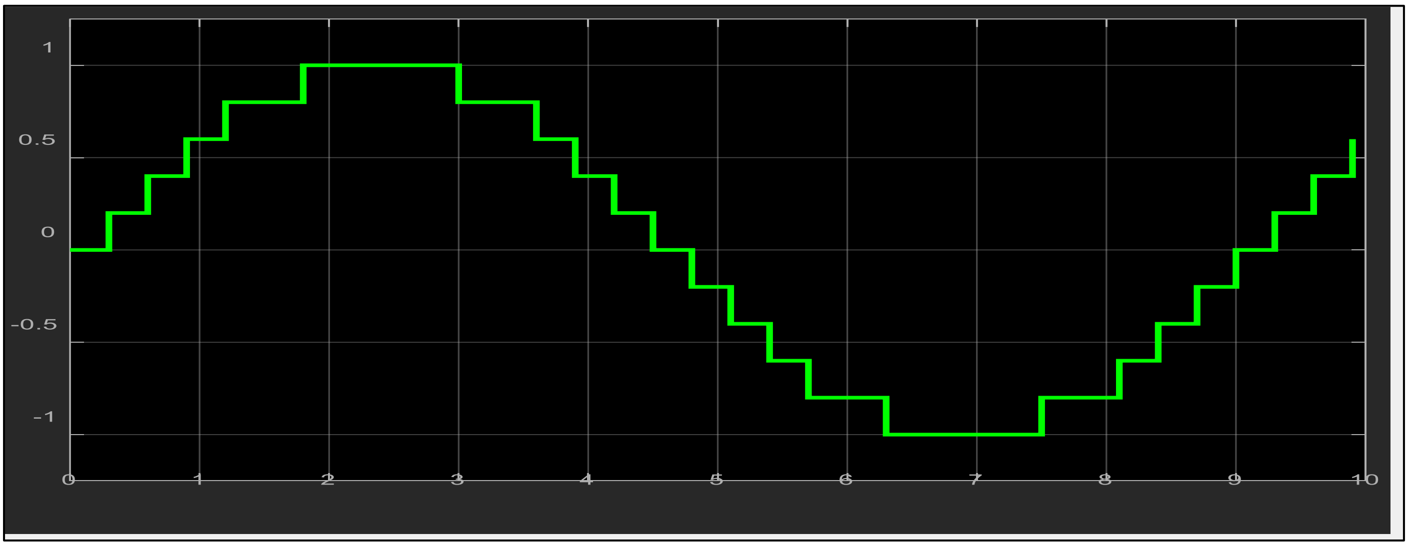

Fig 26: Quantization Output (0.3)

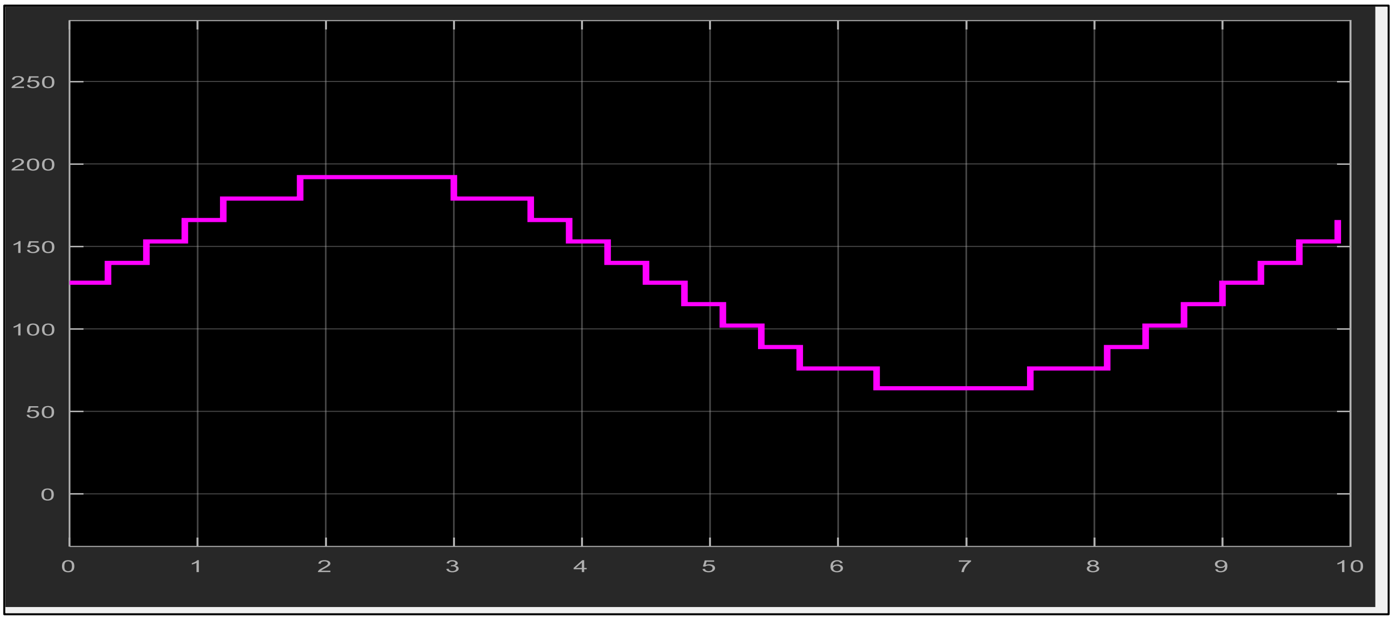

Fig 27: Encoder Output

III. SUMMARY AND CONCLUSION

In this paper study and simulation of ADC is presented. At first define and characteristics of ADC are presented, then different types of ADCS are compared in terms of speed, accuracy and resolution. And then model for ADC is developed with MATLAB/SIMULINK. Finally, this model is simulated at different sampling rate, Quantization level Encoder amplitude in order to show effect of change of these parameters on output results, the output results are outstanding and this model can be useful in teaching purpose in order to give clear picture on operation of ADC and short the gap between the theoretical class and practical field.

REFERENCES

[1]. Suhaib.et.al "Feasibility of Successive Approximation Register ADC in Ultra Low Power Biomedical Applications" International Journal of Engineering and Technology, July 2017.
[2]. N. Shlezinger, R. J. van Sloun, I. A. Huijben, G. Tsintsadze, and Y. C. Eldar, "Learning task-based analog-to-digital conversion for MIMO receivers," in Proc. IEEE ICASSP, 2020, pp. 9125–9129.
[3]. A. Kipnis, Y. C. Eldar, and A. J. Goldsmith, "Fundamental distortion limits of analog-to-digital compression," IEEE Trans. Inf. Theory, vol. 64, no. 9, pp. 6013–6033, 2018.
[4]. J. Guilherme and J. Vital, Logarithmic Analogue-to-Digital Converters, 01 2003, pp. 241–275.
[5]. J. Guilherme and J. Vital, Logarithmic Analogue-to-Digital Converters, 01 2003, pp. 241–275.
[6]. P. Neuhaus, N. Shlezinger, M. Dorpinghaus, Y. C. Eldar, and G. Fettweis, ¨ "Task-based analog-to-digital converters," IEEE Trans. Signal Process., vol. 69, pp. 5403–5418, 2021.
[7]. K. Ogata, Modern Control Engineering. Upper Saddle River, NJ, USA: Prentice Hall PTR, 4th .
[8]. Hemlata Dalmia and Sanjeet K. Sinha "Analog to Digital Converters (ADC): A Literature Review" E3S Web Conf.
[9]. Volume 184, 20202nd International Conference on Design and Manufacturing Aspects for Sustainable Energy (ICMED 2020)