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Performance Analysis of Vedic Multiplier in Signal Processing Applications

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Abstract:- The demand for quick and effective real-time digital signal processing (DSP) applications has increased due to the rapidly advancing technology. Digital signal processors, or DSPs, are essential to several engi- neering specialties. In DSPs, quick multiplication is crucial for operations like Fourier transformations and convolution. One of the fundamental arithmetic processes required by all applications is multiplication. To increase their speed, numerous multiplier designs have been created. Vedic multipliers are among the quick- est and lowest power multipliers compared to array and booth multipliers which are the result of decades of intensive research. The Vedic Multiplier works with sixteen sutras, or algorithms, most of which are for logical processes. Since several of them have been proposed utilizing the Urdhava Tiryakbhyam sutra, they are the fastest and most efficient. This paper's goal is to summarise the many uses of Vedic Multiplier in the broad field of digital signal processing such as image processing, with a focus on the various ways that Vedic Multiplier designs that are now in use have been modified to improve speed and performance metrics.

Keywords:- *Vedic Multiplier, Multiplications, Digital Signal Processing.*

I. INTRODUCTION

"Veda" translates to "storehouse of knowledge." Vedic Mathematics is a traditional branch of mathematics that was rebuilt using the Vedas, a collection of old Indian texts. Its foundation consists of sixteen sutras covering many areas of mathematics, including algebra, geometry, and arithmetic [1]. The most generalised sutra for implementing Vedic multiplier architectures is Urdhva Tiryagbhyam, since both area and delay grow gradually as bit count increases [2]. Vedic multipliers become significant because they may be used to quickly answer difficult mathematical problems by solving them orally [3]. As we can see, the array multiplier takes less computing time because the partial products are calculated individually and concurrently. The time it takes for signals to pass through the gates that make up the multiplication array is known as the delay connected to the array multiplier [4]. Arranging adders is another method to increase the speed of multiplication [1]. The Wallace tree method and the Carry Save Array (CSA) method are the two approaches available for this. In the CSA approach, an adder one bit higher in position receives a carry signal from the processing of each bit individually. Due to the fact that the multiplier's bit count affects the execution time, the CSA approach has certain drawbacks. The carry output signal is passed to the next stage full adder of the same number of bits, and the resulting carry is supplied to the next stage of the full adder. In the Wallace tree method, three bit signals are passed to a one bit full adder, and the sum is supplied to the next stage full adder of the same bit [5]. The Booth algorithm lowers the quantity of incomplete products. On the other hand, huge partial sum and partial carry registers are needed for high speed multiplication and exponential calculations, which call for enormous booth arrays. The least significant half of the result is produced by multiplying two n-bit operands by a radix-4 booth recording multiplier, which takes about n/(2m) clock cycles, where m is the number of booth recoded adder stages. Consequently, this scenario is linked to a significant propagation delay [6]. The Wallace tree multiplier with a modified booth encoding employs the modified booth algorithm to decrease partial products and leverages the wallac tree for faster additions [7-11]. Recently, in a series of research work, it has been claimed that a fast multiplier based on Urdhva tiryakbhyam—a sutra from ancient Indian Vedic mathematics—is outperforms other known multiplies in terms of speed. Vedic multipliers have been used to implement fixed point FIR filters, convolution, digital filters for ECG, EEG signals' denoising, square architecture etc. [7, 13]. Moreover, they are quite helpful in image processing applications where time and space are saved. The practice of applying certain operations to images—such as edge detection, pattern recognition, and sharpening—in order to improve a specific feature or extract important information is known as image processing. For this reason, it is crucial in the domains of robotics, holography, x-ray imaging, mapping, and medical image processing [2, 12-15].

II. BASICS OF VEDIC MATHEMATICS

Vedic mathematics is an age-old method of quick computation that offers a special method of mental calcula- tion with the aid of straightforward guidelines and precepts. The holiness Jagad Guru Shree Bharti Krishna Tirtha JiMaharaj (1884-1960) rediscovered the Veda between 1911 and 1918. After extensive investigation in the Atharva Veda, Swami-Ji claims that the 16-Sutra (Algorithm) and 16-up-sutra (Sub-algorithm) are the founda- tions of all Vedic mathematics [16]. It offers a strong technique that computes all mathematical operations, both simple and complex, swiftly and easily [11]. It gives a quick answer and is more consistent than contemporary mathematics. Because of all the expanding signal processing technologies, essential

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advancements in expedited production have been increasing. It is founded on sixteen sutras that include the topics of algebra, geometry, and arithmetic, among other fields of mathematics. Since modern mathematics is built on numerous mathematical techniques, it is an essential component of technical education in the majority of engineering system design courses. Fast processing speed is required while using the Vedic mathematics algorithm. Furthermore, to implement the Vedic mathematics sutras for DSPs applications, hardware architecture is to be closely observed. The main instrument for signal processing is multipliers which are used in many different applications such as digital filters [12]. Every processing unit's core is its inclusion and multiplication scheme, the effectiveness of which dic- tates the filter's efficiency and operational precision. Additionally, the filter's size slows down the overall process by increasing multiplication. Thus, optimising area and pace is a significant challenge and a conflicting issue in terms of accelerating. Similar to the conventional paradigm, the multiplier measures each resource over a pre- determined period. The literature shows that several multipler algorithims have been developed using different sutras, such as Urdva Tiryakabhyam, Nikhilam sutram, Yavadunam Sutra for DSP applications [3, 14, 15].

III. IMPLEMENTATION OF VEDIC SUTRAS IN SIGNAL PROCESSING APPLICATION

➢ *In this Section, the Basic Sutras which are Frequently used to Implement DSP Applications will be Discussed.*

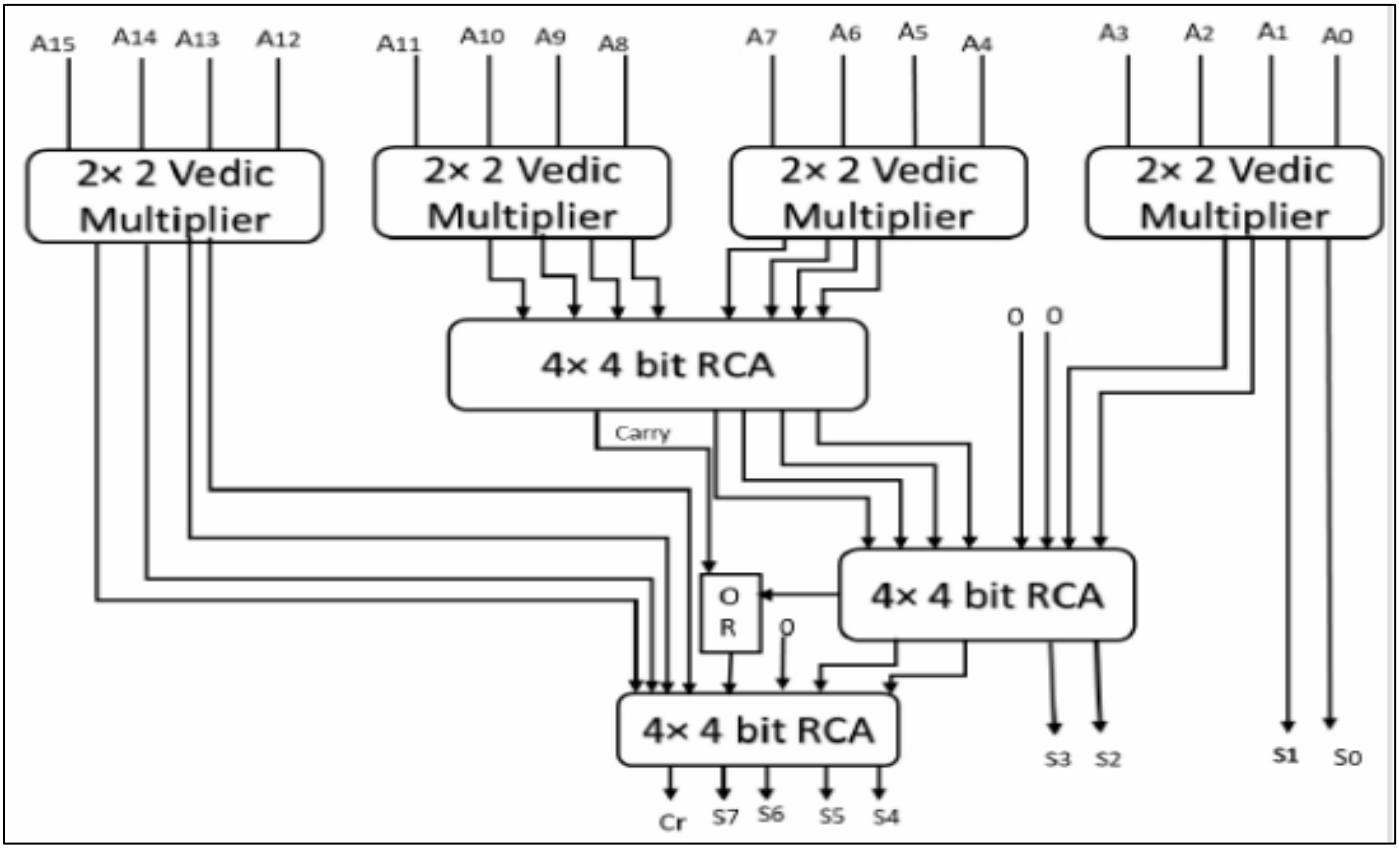

Fig 1 4x4 Binary Multiplication

- *Urdhava Tiryakbhyam*

The foundation of Urdhava Tiryakbhyam is a revolutionary idea that allows for the simultaneous generation of all partial products. This approach is shown in Fig. 1 as a 4x4 binary multiplication. This multiplier has been developed by small units of 2x2 Vedic multipliers, which are computing in parallel [2].

Further, any N x N bit multiplication can be accomplished using the generalised method. The partial products and their sums are computed in parallel, therefore this is independent of the processor's clock frequency. Overall, this is advantageous since it lessens the requirement for microprocessors to run at progressively higher clock speeds. A processor's running frequency and switching instance count are positively correlated. This leads to increased power consumption and heat dissipation, raising the operating temperature of the gadget. It's expandability is an additional benefit. Because it has a regular structure, increasing the input and output data bus widths will simply improve the processing power. It's regular structure allows for easy layout in a silicon chip and optimal area consumption. Compared to other multipliers, the gate delay and area rise extremely slowly as the number of input bits increases. As a result, the Urdhava Tiryakbhyam multiplier uses less time, space, and energy.

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- *Nikhilam Sutram*

Utilising Nikhilam Sutra for multiplication, the table below illustrates how Nikhilam Sutra can be used to accomplish addition and shift operations, as well as two-three digit multiplication, with just one multiplication. Table I 107 * 109 Multiplication using integer base difference Multiplier of 107 (100-107) = 7 109 (100-109) = -9 Factor The result is 11663. (107-(-9))=(109-(-7))=116 (-7)*(-9)=63 116 63 In the Karatsuba algorithm, multiplication is necessary for step 4, while multiplication is required for step 9 in the traditional technique. The following is the underlying idea of the Nikhilam Sutra: If n=x+b and m=x+a is the multiplicand, and x is the closest base, then m*n= (x+a)*(x+b)=x(x+a+b) + ab.

- *Yavadunam Sutra*

The Yavadunam sutra can be used to square a number, which translates to imply, "write the square of the deficiency and determine the deficiency, lessen the deficiency from that number" [3]. The Yavadunam sutra's up-sutra is called Yavadunam Tavadunikrtya Vargancha Yojayet (YTVY). This formula's unique requirement is that it can only be used to find the square of any integer that is closer to the bases of powers of 10, that is, 10, 100, 1000, 1000,...The Yavadunam sutra of Vedic mathematics can be used to get the square of a number by following these steps. Step 1: Use the closest base to identify the deficit. Step 2: Place the shortfall on the right side and square it. Step 3: Increase or decrease the amount by the deficiency. Step 4: The outcome is equal to [|Number - Deficiency|+ carry over] & [Deficiency Square]. The discrepancy between the base and the input to be squared is known as the deficit. The closest base of powers of 10 for the number "7" is "10." The current 7 deficit is 10-7 = 3. The closest base of powers of 10 for the number 997 is 1000. As of right now, 997's deficit is 1000 -997 = 3. However, this sutra works only when the integer that needs to be squared is closer to a power of 10. Furthermore, the Yavadunam sutra does not currently have a conventional architecture. Because the input comes from a range of sources, designing a specific architecture is a difficult undertaking.

IV. PERFORMANCE ANALYSIS

Research in the last decade shows that Vedic multipliers have improved the conventional designs of DSP applica- tions. In [17], it is claimed that FIR and IIR filters of various orders are designed and implemented using vedic multiplier. Further, these filters are used to denoise noisy ECG signals. The digital filters with vedic multiplier results outperform the conventional filters in terms of hardware and power consumption. In another research work, Kerur et. al observed that 8-bit vedic multiplier achieves higher speed by reducing gate delay by factor of 24% compared to array multiplier and around 18.2% compared to booth multiplier [18]. DSP processors implemented using Vedic multiplier in [1] also claim that it is highly effcient in terms of speed. Its parallel and uniform structure makes it simple to realise on silicon as well. Similarly, Deepa et. al have presented that Yavadunam vedic multiplier outperforms the Array multiplier by 56.88%, the Braun multiplier by 39.01%, the Shift and Add multiplier by 91.46%, the Wallace multiplier by 31.17%, the Dadda multiplier by 13.46%, the Urdhava multiplier by 65.33%, and the Nikilam multiplier by 23.57% in terms of area delay product [3]. In one another research work, Meenakshi et. al have proposed vedic notch and peak filters (VNPF) which are compared to existing filters. The proposed designs are consuming less power and occupying small hardware compared to conventional filters [19]. The above mentioned research works show that the multipliers implemented with vedic sutras perform better compared to conventional multipliers. Further, including vedic multipliers in any DSP application improves the overall hardware implementation in terms of power consumption, area and speed.

V. CONCLUSION

A concept of symmetric computation can be found in Vedic mathematics. Numerous mathematical concepts, including calculus, geometry, trigonometry, and fundamental arithmetic, are covered in Vedic mathematics. When it comes to manual computations, all of these techniques are incredibly effective. Regarding speed, the suggested Vedic multiplier turns out to be really effective. In terms of speed, the suggested Vedic multiplier turns out to be very effective. Its parallel and uniform structure makes it simple to realise on silicon as well. The primary benefit is that the delay grows gradually with the number of input bits.

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