ISSN No:-2456-2165

Reset Noise Sources and Suppression Strategies for CMOS Image Sensors

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Abstract:- Noise in CMOS image sensors (CIS) has always been the key factor to compete with its counterpart technology of charged coupled devices (CCDs) in industrial and scientific applications. In the wake of that, a lot of research has been carried out broadly targeting the category of temporal and spatial noise. Noise suppression strategiesfor both these categorieshave experienced significant change in its design, especially after the year 2000. While the earliermethods of temporal noise removal including local oxidation, transistor sizing, accommodation of pinned photodiodes etc. majorly targeted the restructuring of sensor's pixel; modern strategies focus on off-chip noise cancellation schemes with variety of sampling and reset methods.This paper addresses the study on resent noise source and its suppression strategy.

I.INTRODUCTION

In last two decades, CMOS image sensors (CIS) have received special attention of researchers, because of their very promising performance compared to the other competing technologies of micro photodiodes and charge-coupled devices (CCDs). Low power operation, greater processing speed, and flexibility in design are some of the standout features of CIS, which makes them suitable for modern biomedical and scientific imaging applications. The only bottleneck in CIS performance is noise that overshadows all these advantages [1–3]. Identifying the need of noise correction, distinguished researchers across the globe have performed exhaustive research having targeted the various noise sources, as listed in table 1.

	Semiconductor device noise	Circuit noise
Temporal noise	Random telegraph noise (time domain)	Reset noise
	Low frequency noise/ flicker noise (frequency domain)	Readout noise
	Thermal noise	Integration noise
	Shot noise	Source follower noise
	Dark current noise	
Spatial noise	Fixed pattern noise (FPN)	
	Dark signal non uniformity (DSNU)	Photo response non uniformity (PRNU)
		Pixel, Row and Column FPN

Table 1: Sources of noise in CMOS image sensor

Among the various noise sources present in the CIS, this paper focuses on cause-effect study of circuit noise source specifically the reset noise source and its suppression strategy.

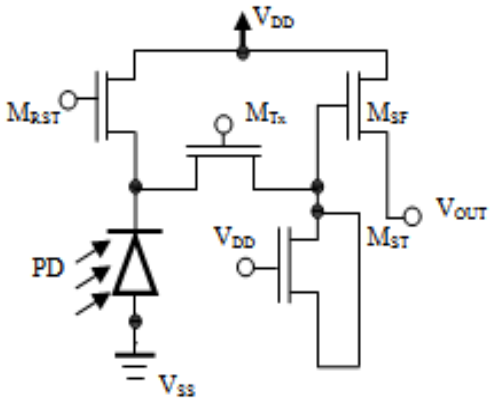

Fig. 1: Circuit diagram of CMOS image sensor

II. BASIC FUNCTIONING OF CMOS IMAGE SENSOR

The 4T-CMOS imager consists of a photodiode which is pulled up towards V_{DD} through NMOS transistor load (M_{RST}), whose gate is connected to reset signal (Fig.1). The value sampled is actually stored on the storage transistor (M_{ST}) whose gate is connected to bias voltage V_B. This transistor here is serving two purposes, acting as a buffer to pass on the value to source follower amplifier (M_{SF}) and also for storing the noise value as MOScap. The TX signal controls the value to be stored using an NMOS pass gate (M_{TX}). The voltage stored is buffered through a source follower amplifier. The readout chain consists of simple CDS circuit with 2-stage CMOS-OPAMP for better noise and improved gain performance.

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III. CAUSE-EFFECT OF RESET NOISE SOURCE IN CMOS IMAGE SENSOR

In order to understand the development in noise suppression strategies for reset noise, it is important to highlight the cause-effect of this source. Temporal noise due to reset transistor's non linearity also contributes as a fundamental limit on the performance of CIS. On the other hand read noise occurs while reading the information from row select transistor and outside circuitry (generally ADC). The lower the read noise level, the lower is the probability of detecting the minimum number of signal electrons.

Resetting of sense node prior to charge accumulation cycle causes reset noise to occur. It dominates in low illumination conditions [4]. Mathematically it is expressed as [5]:

$$Un=\sqrt{\frac{KT}{C}} \qquad (3)$$

where Un is r.m.s. noise voltage, K is Boltzmann constant in joules/Kelvin, C is the sense node capacitance in farad and T is the ambient temperature in Kelvin.

It is important to accurately measure reset noise specially with downscaling of CMOS technology. It was found that for high illumination the temporal noise value due to reset noise remains the half of commonly quoted value and shot noise prevails. But for low illumination the reset noise dominates [4].

IV. SUPPRESSION STRATEGIES FOR RESET NOISE IN CMOS IMAGE SENSORS

Considering reset and readout noise as major limitations two main streams of research have been recognized; one stream is related to the introduction of a charge transfer mechanism to allow CDS to be performed on-chip and other is to reduce the noise by modifications in CIS design.

A. Introduction of charge transfer mechanism:

In the standard design of 3T pixel CIS there is no other capacitor than the sense node available which can restore the reset noise values. This is the reason that restricts the in pixel cancellation of reset or kTC noise in 3T APS. Therefore, researchers in early days tried to develop the schemes which could allow the charge transfer mechanism so that sampling methods can be applied.

Buried photodiode was one of the earlier structures explored for the charge transfer mechanism [6], [7]. It has a shallow implant which forces the charge carriers away from the surface traps of Si or SiO2 which are the main contributors of leakage current and noise in CIS. So use of buried photodiode allows the sampling technique like CDS to be implemented before and after the charge transfer. Later on a photo-gate as a detector with double polysilicon layers was used to transfer the charge stored across it to the previously reset floating node, thereby allowing the CDS to operate [8]. However the approach required the double polysilicon structures which are rare used CMOS technology. Also the photo-gate CIS has the disadvantages of lower fill factor and lower quantum efficiency with incomplete charge transfer.

In the process of transferring the charge it was later realized that use of PPD could better serve the purpose [9], [10]. Moreover such structures also don't require any double poly structures, hence can be readily available and adopted. The original idea was to suppress the leakage current by introducing the surface implants restraining the surface currents, but addition of transfer gate helped in transfer of full charges. The charge transfer concept using PPD is shown in Fig. 2 (a).

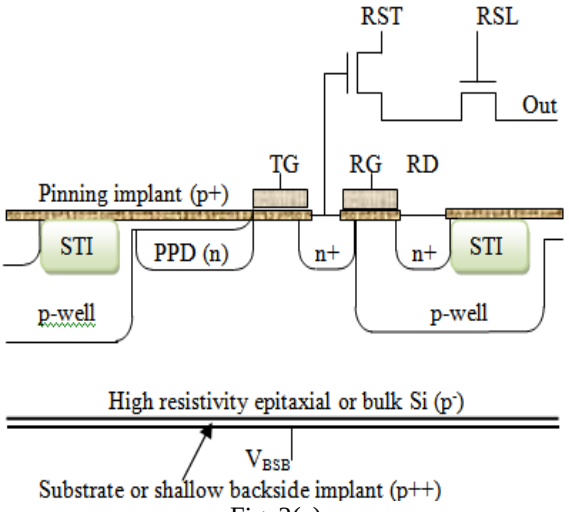

Fig. 2(a)

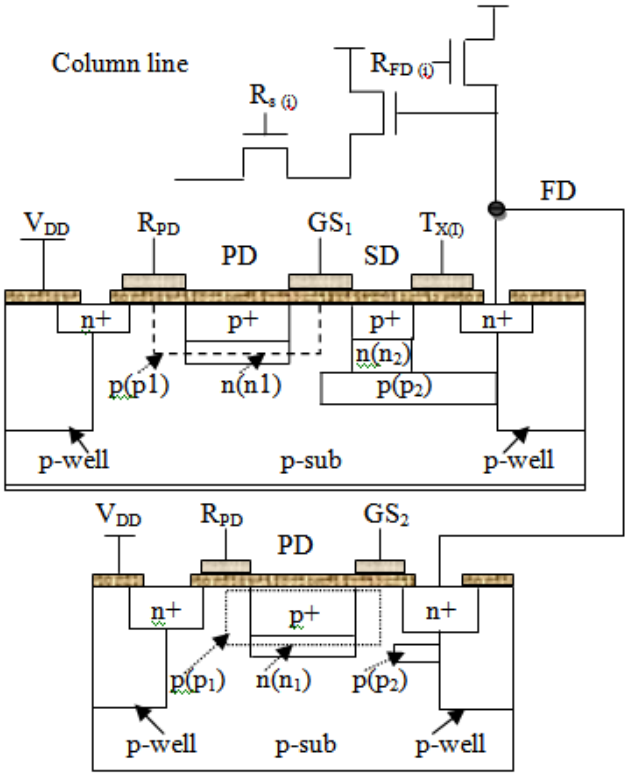

Fig. 2(b)

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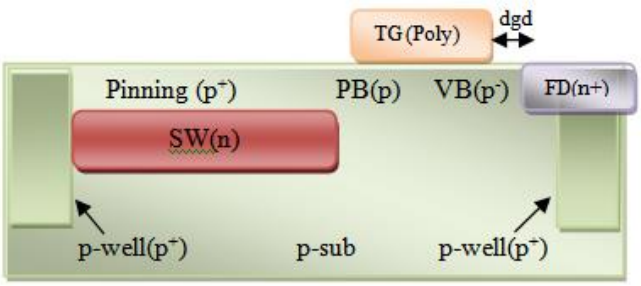

Fig. 2(c)

Fig. 2: Charge transfer mechanisms through different PD designs. (a) Basic structure of Pinned Photodiode (PPD). (b) Two stage charge transfer mechanism using two PPDs responsible for photoelectron conversion and charge storage respectively. (c) Cross-sectional schematic view of PPD-PG pixel.

It is important to understand that not all buried PD are PPDs but all PPDs are by necessity buried PDs. In other words buried PD avoids pinning of the Fermi level at its surface.The disadvantages of utilizing PPD sensors are the significant modification in CMOS technology and higher reset voltage for complete charge transfer. A contrary theory related with charge transfer noise behaviour was presented in [11]. This investigation revealed that charge transfer noise and lag in buried photodiode behaved as shot noise unlike the conventional theory of (KTC) ½.

The method of two stage charge transfer utilizing two PPDs was presented in [12]. Two PPDs using different depth potential wells were used in the approach with the objective of photoelectron conversion and charge storage respectively. This method of two stage charge transfer introduced the dual doping and shielding technique, as shown in Fig.2 (b). The purpose behind the dual doping technique is to improve the charge transfer efficiency, by creating the adequate potential difference between the PPDs. On the other hand the shielding structure utilized helped in achieving the higher shutter efficiency for storage PPD.

The discussion over charge transfer schemes in CIS will remain incomplete without including the contribution of the methods of reducing the capacitance of FD node, especially in quanta CIS [13]. The overlapping capacitance between the TG and FD has the noticeable contribution in forming the FD capacitance, significantly reducing the CG of the CIS. Understanding the potential of noise reduction by increasing the CG through reduction of the FD node capacitance, number of groups has worked recently in this area, with the target of modifying the methods of charge transfer inside the pixel. All these methods are based on utilizing the pinned photodiode pump gate (PPD-PG) pixel. A vertical transfer pump-gate with distal FD utilizing the concept of virtual phase carrier transfer is covered in [14–16]. Extension of the p+ pinning layer to the edge of FD allowing the complete depletion of the channel between TG and FD [17], [18], and a self aligned source/drain structure [19], [20] have been some of the recent methods adopted by researchers for reduction of FD node capacitance. Lower dynamic range and poor fill factor on the cost of higher CG remained as challenge in the implementation of these methods, especially in front illuminated devices. As back illuminated CIS follows different strategy for charge transfer, PPD-PG approach doesn't belong to them.

Fig. 2 (c) depicts a method of obtaining the higher CG by reducing the FD junction capacitance, with cancellation of channel stop implantation under FD. It helped in reduction of p-type doping concentration under FD reducing the capacitance, thereby increasing the CG and lower readout noise [21]. The proposed method also applied measures for improved dynamic range and fill factor of the CIS.

B. Modification in image sensor's design:

Hardand soft reset schemes have been employed frequently for suppression of reset and FPN noise in CIS. In soft reset schemes both gate and drain of the reset transistor is kept at the same potential using the sub threshold current, resetting the sense node. Whereas in hard reset method the reset transistor's channel can be observed as a pure resistance R, as it operates in the linear region. Hard reset methods are more prone to the anomalies of increased reset noise and lower saturation levels, however soft reset schemes are better in reducing the reset noise but have problems of image lag and response non linearity[22–24].

The active reset method was one of the earliest soft reset methods used to reset the sense node [25]. The scheme is shown in Fig. 3(a). Initially pulsing of Vpr pulls the Vpd to ground. When Vg approaches to Vdd, M5 turns on resulting in gradual rise of Vr, which then turns on M1. Vpd follows Vr and after some time Vpd overshoots Vr. The output of amplifier drops and M1 turns off. And finally with fall of Vg, M5 turns off. The features of band limiting and capacitive feedback of this scheme helped in reducing the reset noise without introducing any image lag. However, longer reset period, accommodation of extra transistors resulted in increased pixel area and power consumption.

Unlike CCDs, application of on-chip CDS is not feasible for CIS. Since CIS works on read first reset later mode, hence the incorporation of CDS schemes is only possible in off-chip mode [26]. However, off-chip CDS schemes cost the higher flicker, white noise, complexities and full-frame buffer. Therefore a number of other reset strategies, including the tapered reset method, capacitive divider circuits suppressing the front end reset noise were explored afterwards [27], [28].

Rectifying the disadvantages of conventional active reset scheme, later, a column based active reset scheme with the accommodation of single transistor was introduced in the CIS circuit [29]. With the least impact on QE and fill factor, this method proved a good alternative of active reset scheme. The only reported problem was reduced signal handling capacity due to the early reset of sense node than that of the standard pixel cell of CIS.

Identifying the shortcomings of hard and soft reset schemes, flushing reset was the next advancement observed that provided the alternative for reset noise suppression [23]. Schematic of flush reset circuit is shown in Fig.3 (b).The flush operation completely erases the pixel memory, eliminating the non linearity and image lag, and soft reset

ISSN No:-2456-2165

ensures the lower noise and large saturation of the signal. Hard reset is performed by simultaneously triggering the øreset, øflush (logic high) and ørow-sel (logic low), causing M_{FR} transistor to be turned off and PWR-BUS gets disconnected from Vdd. This makes the current to be steered on different path formed by M_{Fdrop}, $M_{FR\text{-}cut}$, and $M_{FR\text{-}Load}$. After the hard reset, soft reset is accomplished by pulsing of the ørow-sel to logic high and øflush to logic low.

Further improving the reset schemes in terms of signal swing [30], a method of dynamic reset level control was proposed in [31]. The concept of dynamic reset level control utilizes the weak inversion region of pixel's operation and column parallel comparator (Fig.3(c)). After conventional reset operation, the reset current discharges the photodiode's node to the level of reference voltage. Because of shunting of reset current by pixel diode capacitance, the PSD of noise gets shifted into the low frequency region. Hence adjusting the pixel reset to reference level for each column comparator, results in a reset noise reduction in both the pixel and read out circuitry.

An approach of tapered reset system with the concept of distributed negative feedback reset [32], presented an interesting approach of different reset and readout modes. Reset mode utilized the 6-transistors for active reset followed by 3-transistors in readout mode. The method achieved good image lag performance with reset noise reduction. However, maintaining the enough tapered reset time, which could control the small parasitic leakages was the only challenge.

Schmitt trigger based auto reset scheme, extended pseudo flush reset scheme were some of the other techniques adopted for resetting the sense node of CIS [33], [34].

In one of the recent advancements of reset circuit design to lower the read noise, a method of reset gate less CIS was proposed in [35]. The schematic is shown in Fig.3 (d). By eliminating the parasitic capacitance, the FD reset was performed through capacitive coupling between FD and source follower output, hence named as bootstrapping reset. Low supply voltage for FD reset was the main feature of this approach, making it suitable for high resolution and high readout pixel designs.

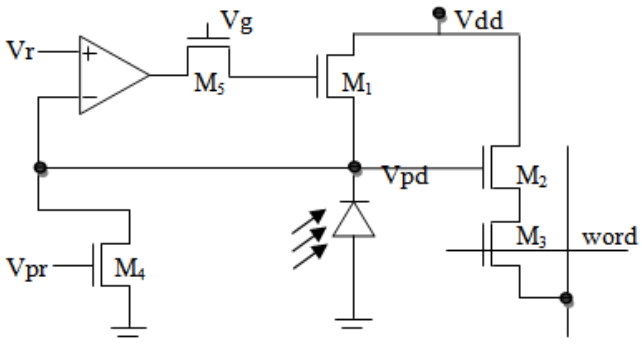

Fig. 3(a)

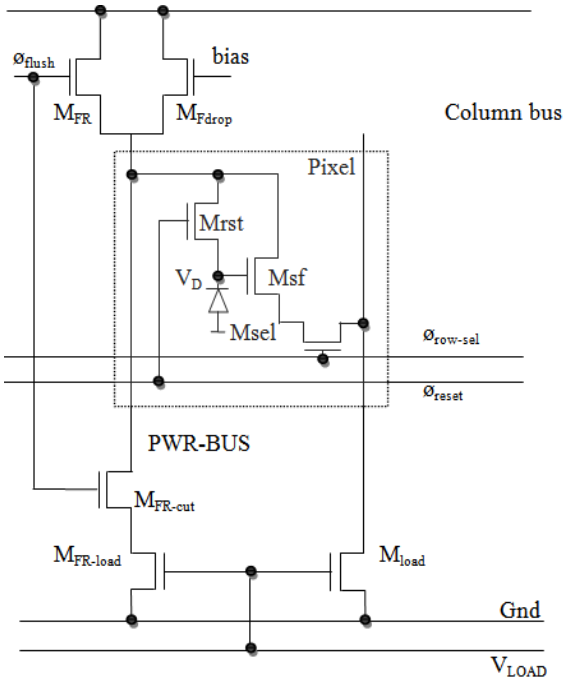

Fig. 3(b)

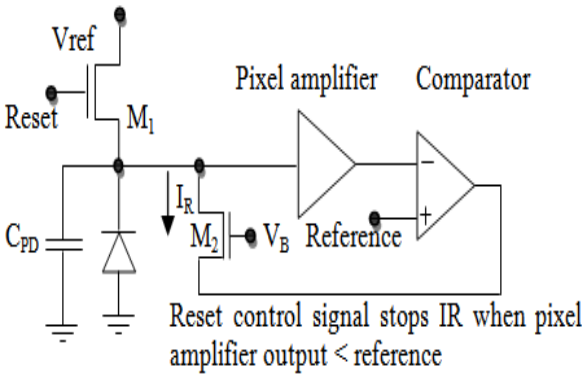

Fig. 3(c)

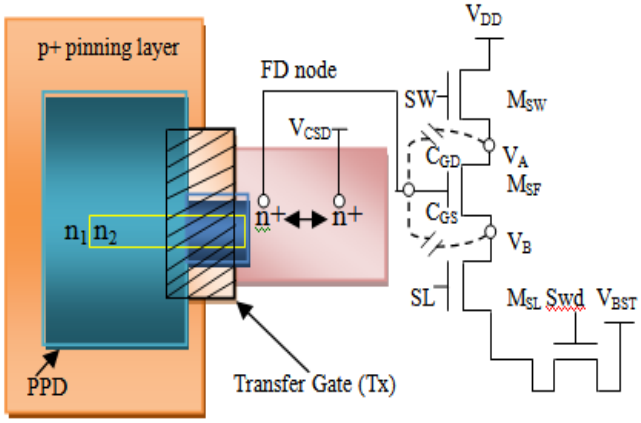

Fig. 3(d)

Fig. 3: Different strategies of reset circuitries(a) CIS with active reset scheme, (b) CIS with reset-assist (flushed reset) circuit, (c) Concept of dynamic reset level control system,(d) Reset-gate-less pixel with bootstrapping reset scheme.

ISSN No:-2456-2165

V. CONCLUSION

Suppression strategy categorized in two types, one is modification in pixel design and other is modification in reset circuitry for removal of reset noise source in CMOS image senor has been discussed in detail in this paper. Comparative study of noise removal strategies gives an impression that the major challenge is to maintain the efficacy of CIS with suppression of non-idealities. The methods of BIST and DFT can be useful in bridging the gap between enhancement in performance and removal of noise for CIS [36-39]. The information provided in this paper will definitely help the researchers and engineers working with CIS to understand and analyse the cause and effect of reset noise sources along with the suitability and acceptability of specific remedial technique before making any choice for any application.

Type of noise	Suppression method	Drawback/Trade-off
Circuit noise (reset and readout)	Charge transfer through depletion of channel between TG and FD [80-83]	Lower dynamic range and poor fill factor
	Active reset scheme [88]	Longer reset period, Increase pixel size and power consumption
	Off-chip CDS scheme [89]	Higher LFN, complexity and white noise

Table 2: Trade-offs and drawbacks of popular noise suppression methods

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